

# TOPIC: STORE AND FORWARD

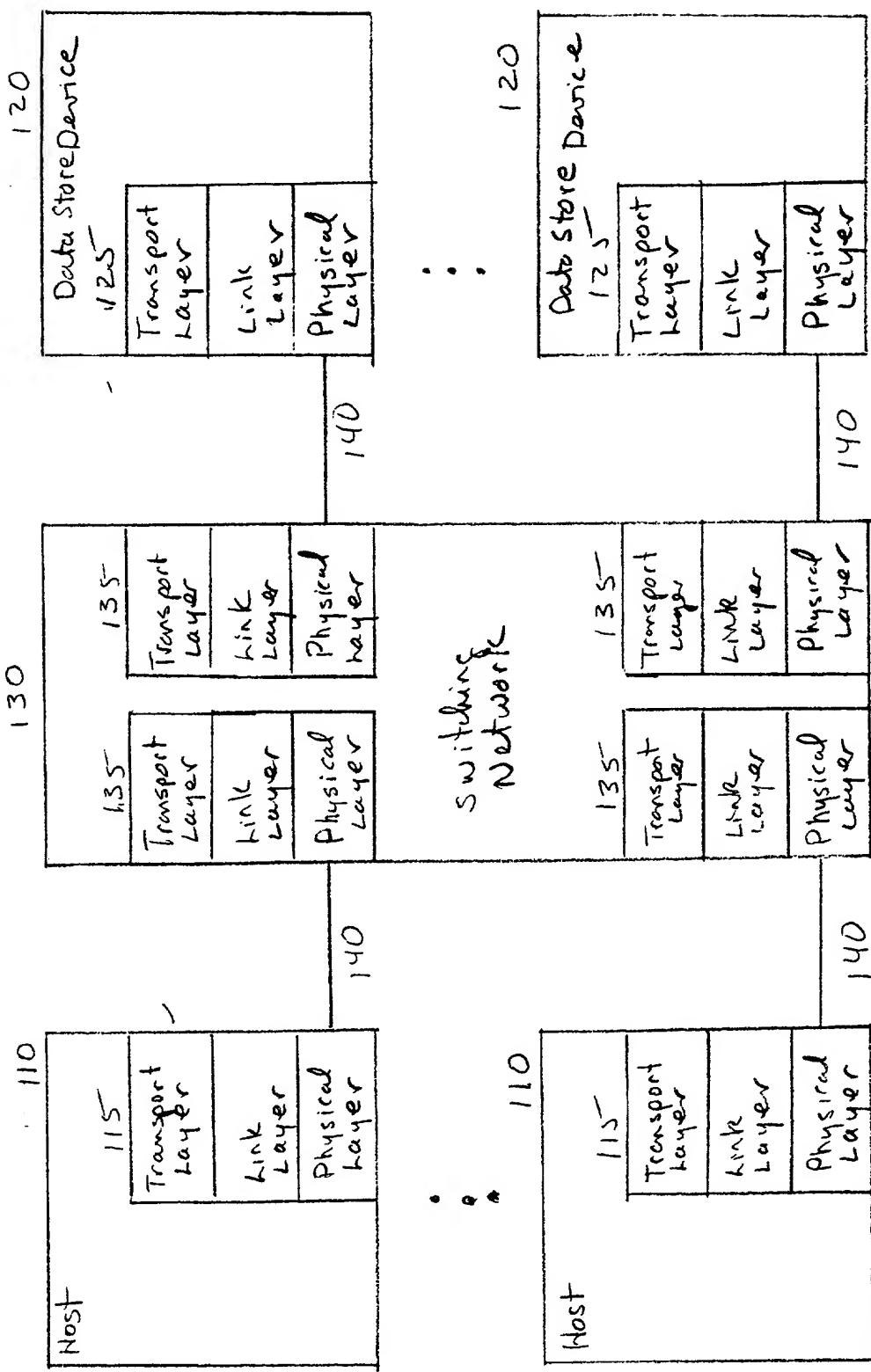


Fig 1

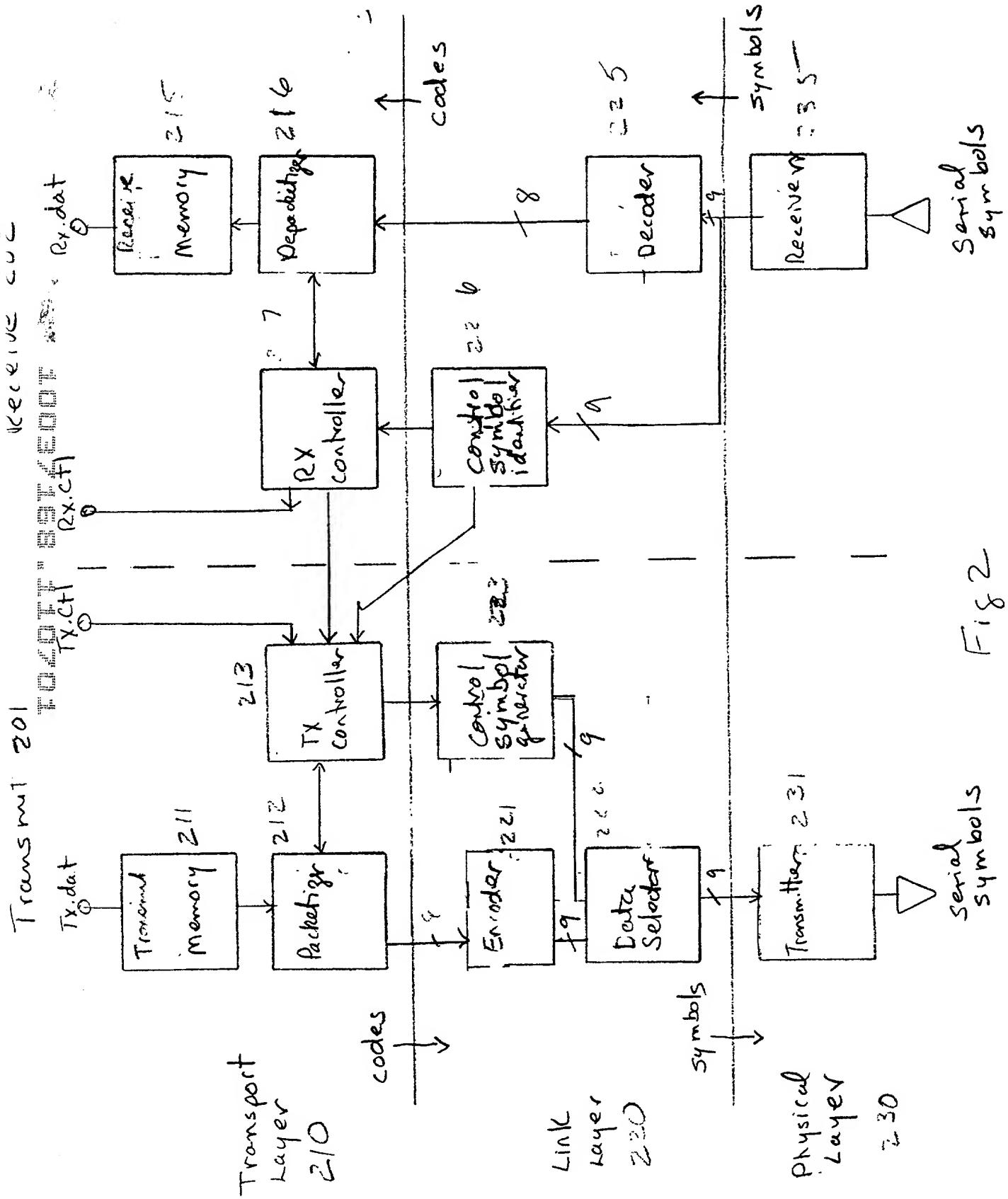


Fig 2

Serial symbols

Physical Layer 230

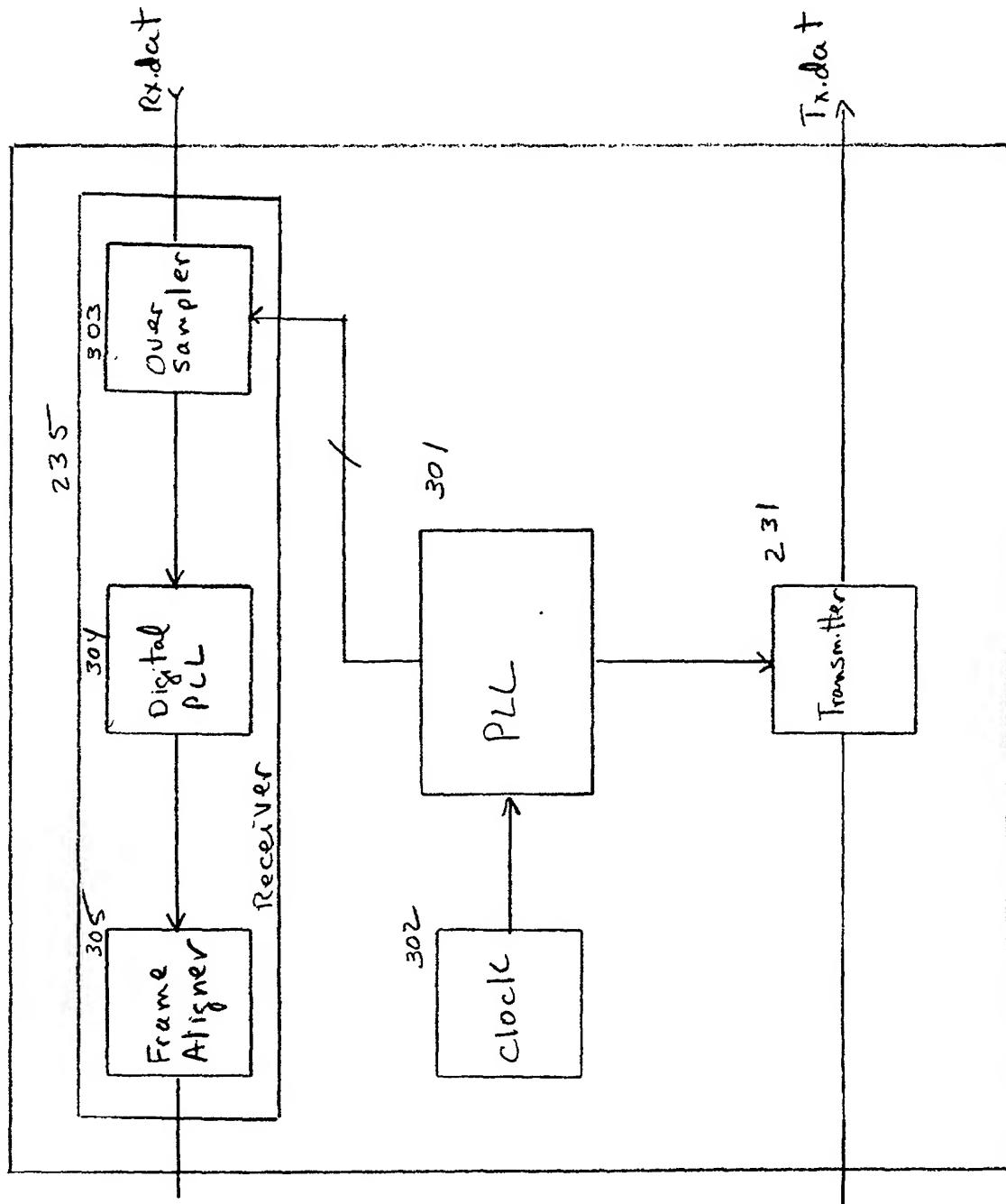


Fig 3

# Packet

400

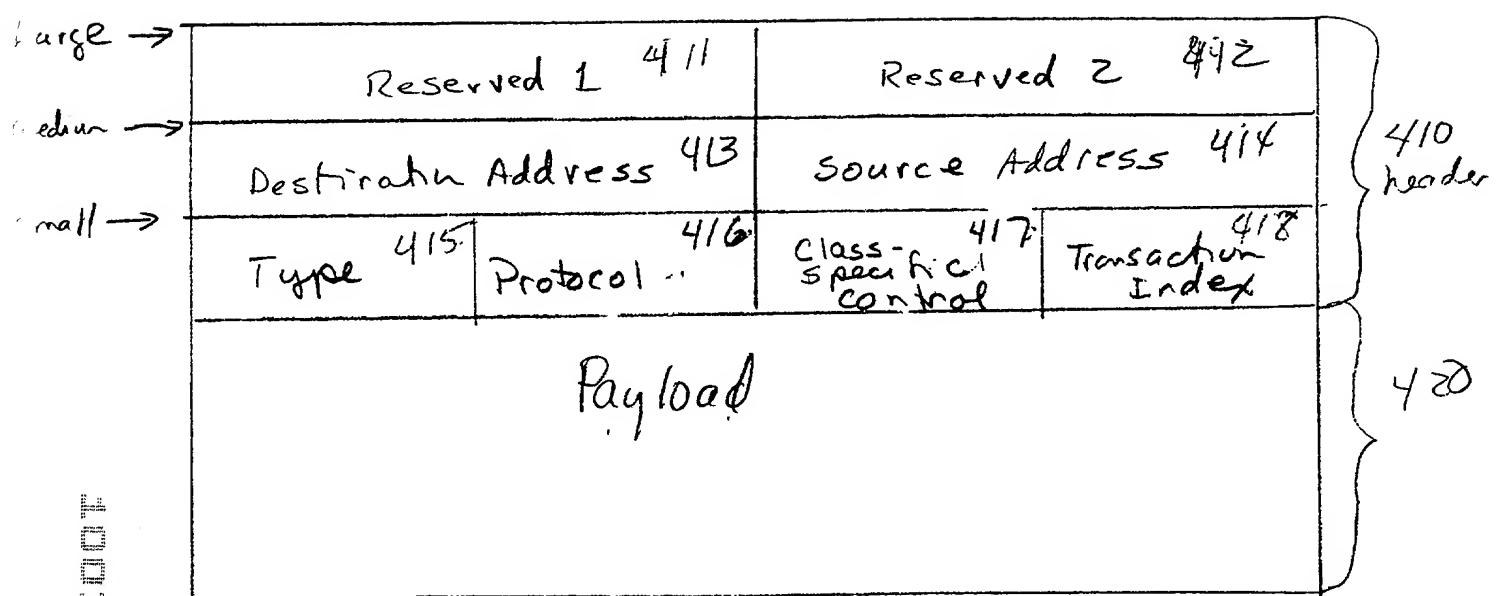
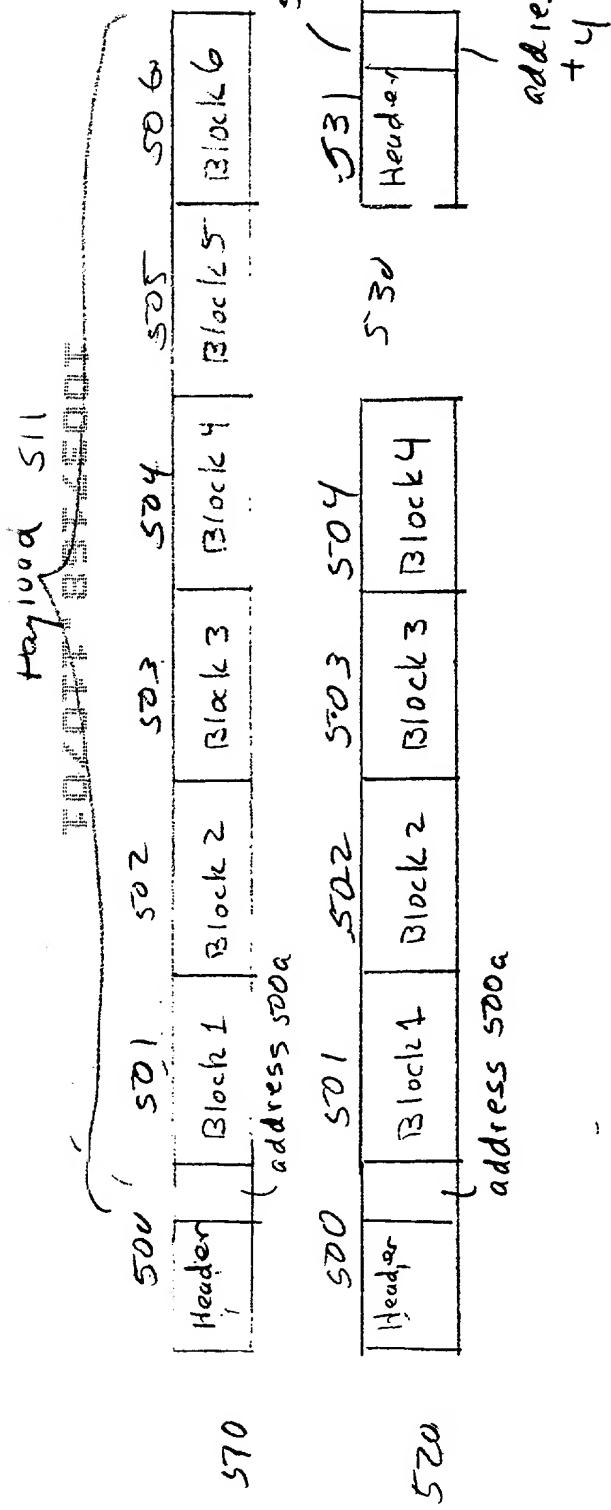


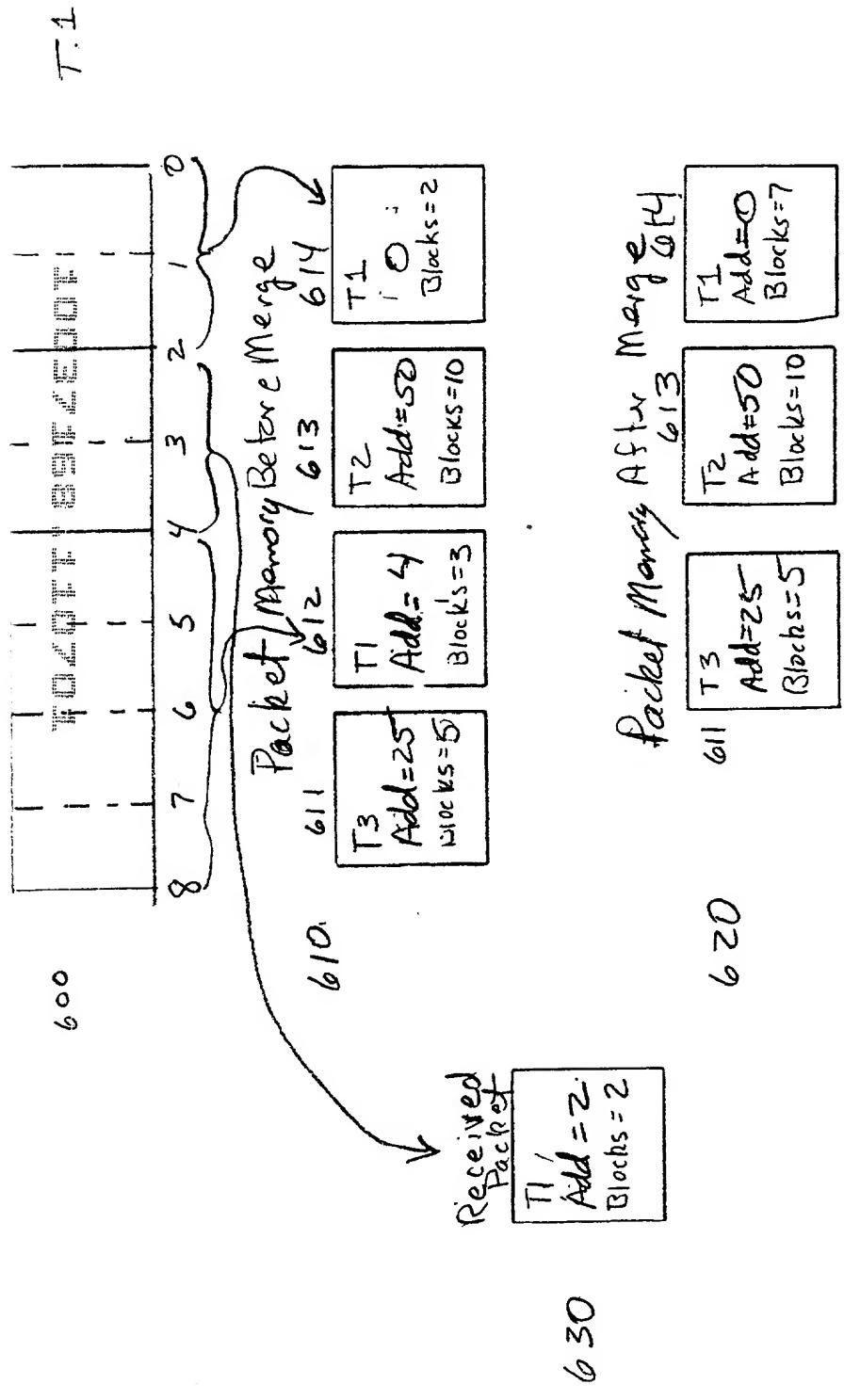
Fig 4

# ~~Memory Organization~~



address  
+4

F. 15



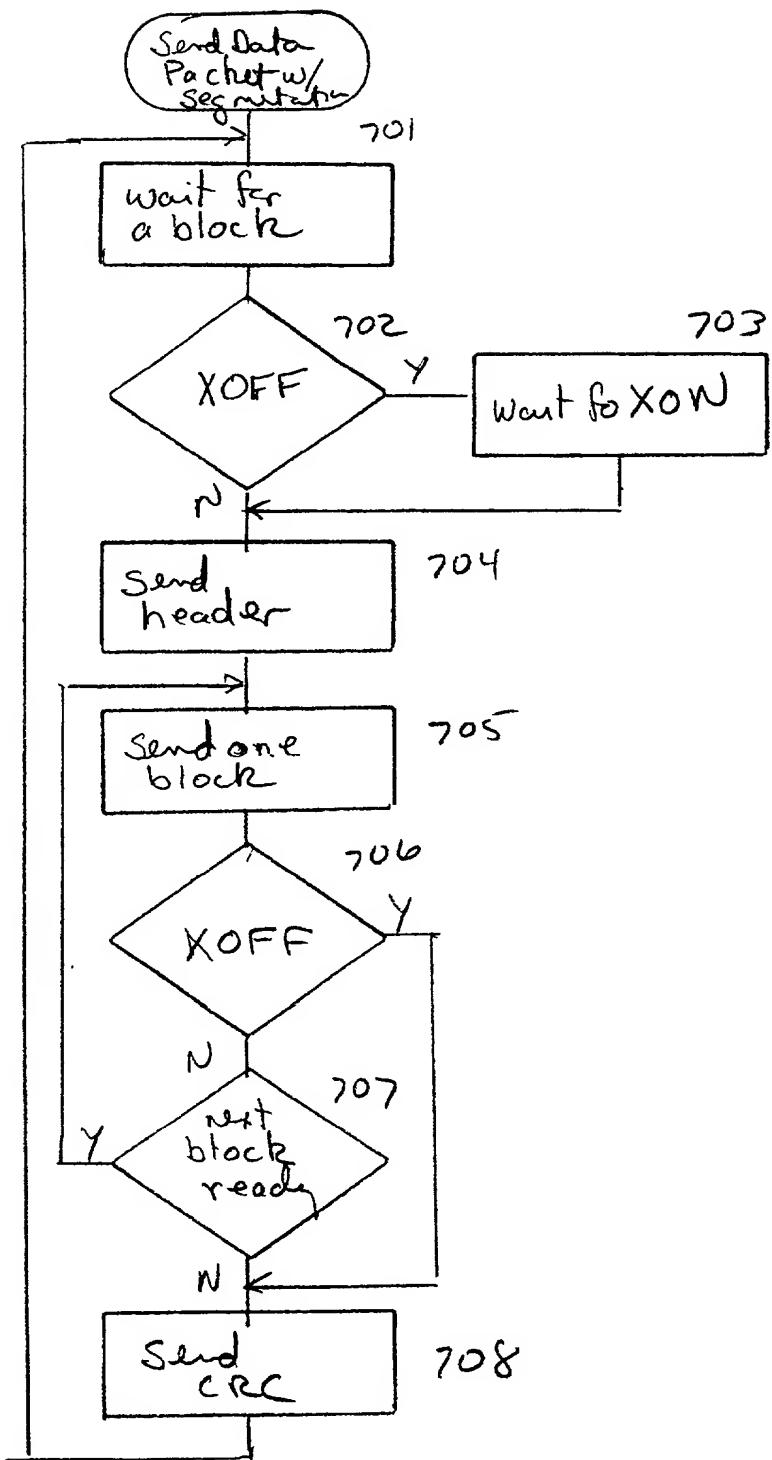


Fig 7

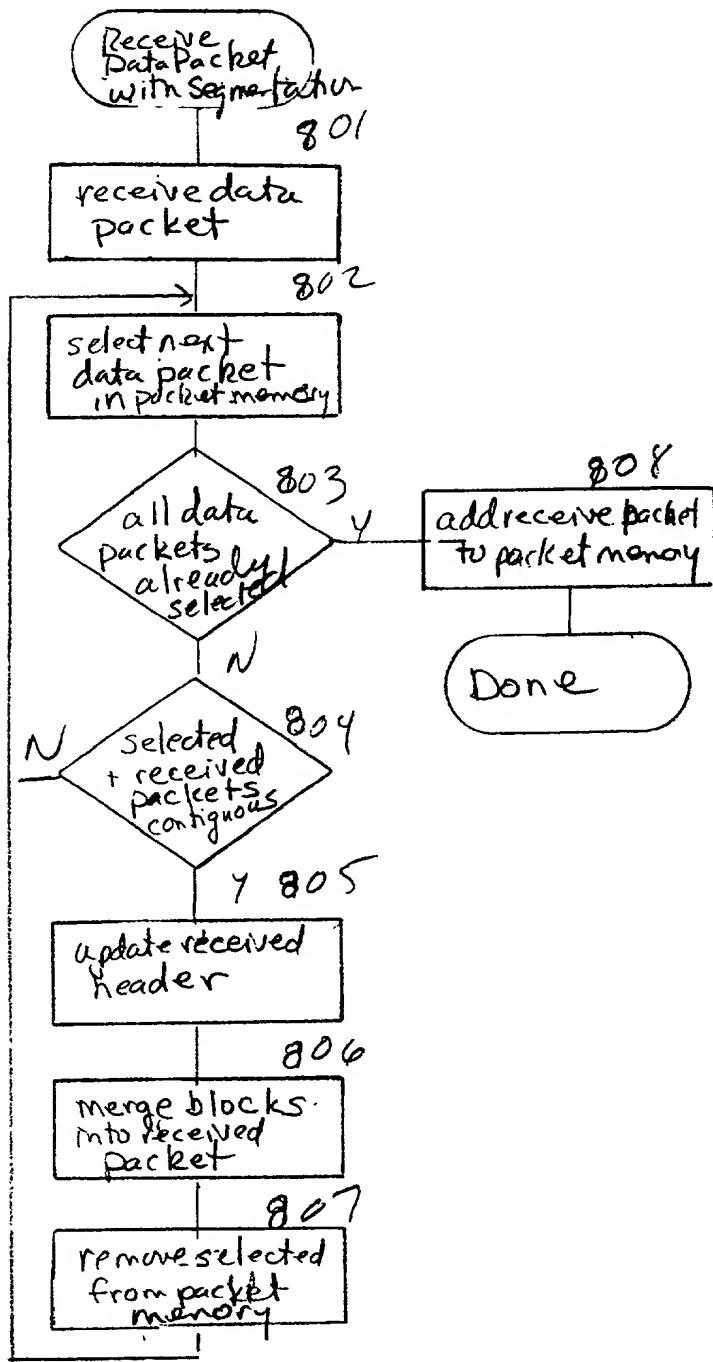
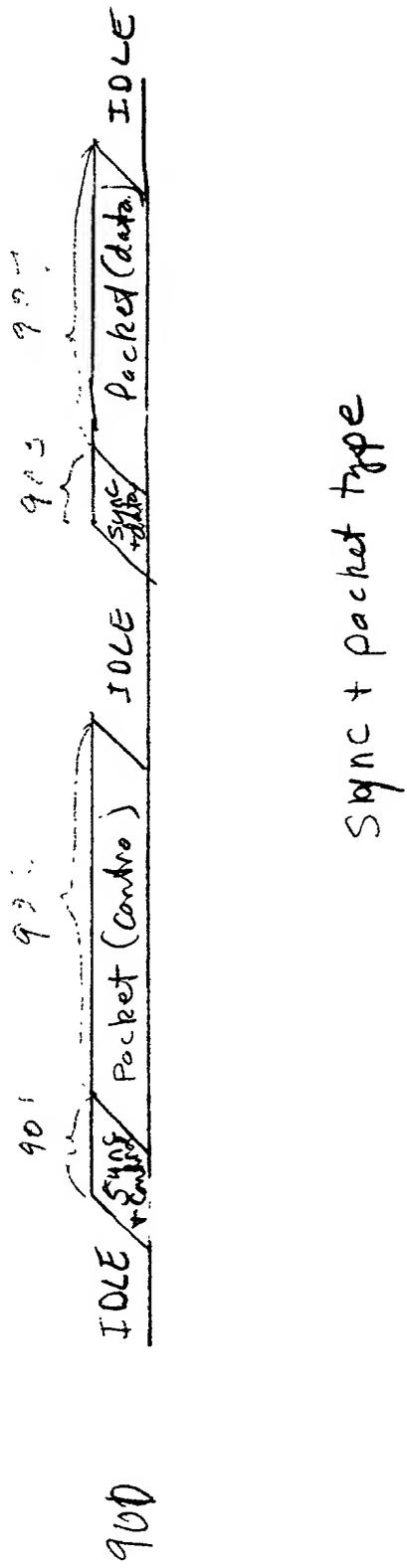


Fig 8

Fig 9A Sync + packet type



Sync + packet type

Fig 9A

FIG. 10

Fig 9 B

Fig

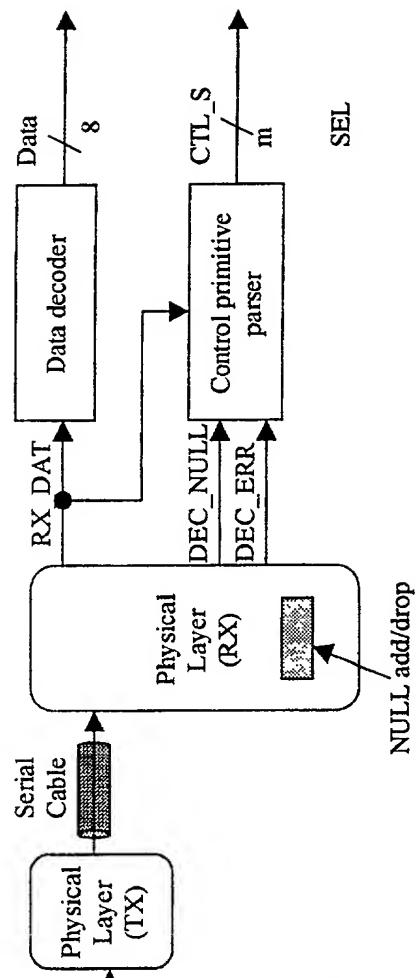
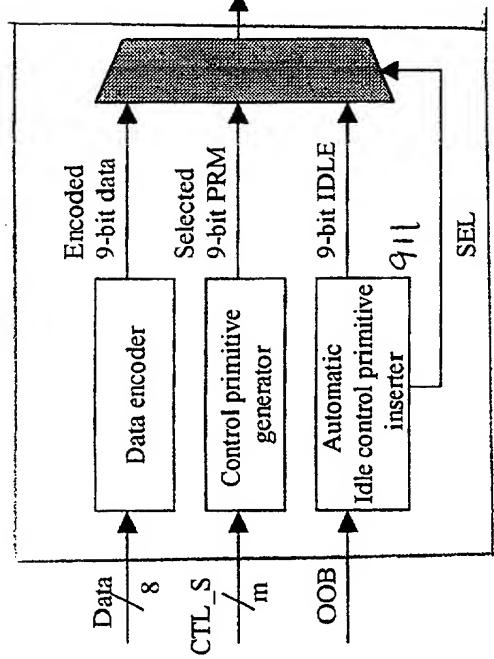


Fig 8.9C

### Packet Memory 211

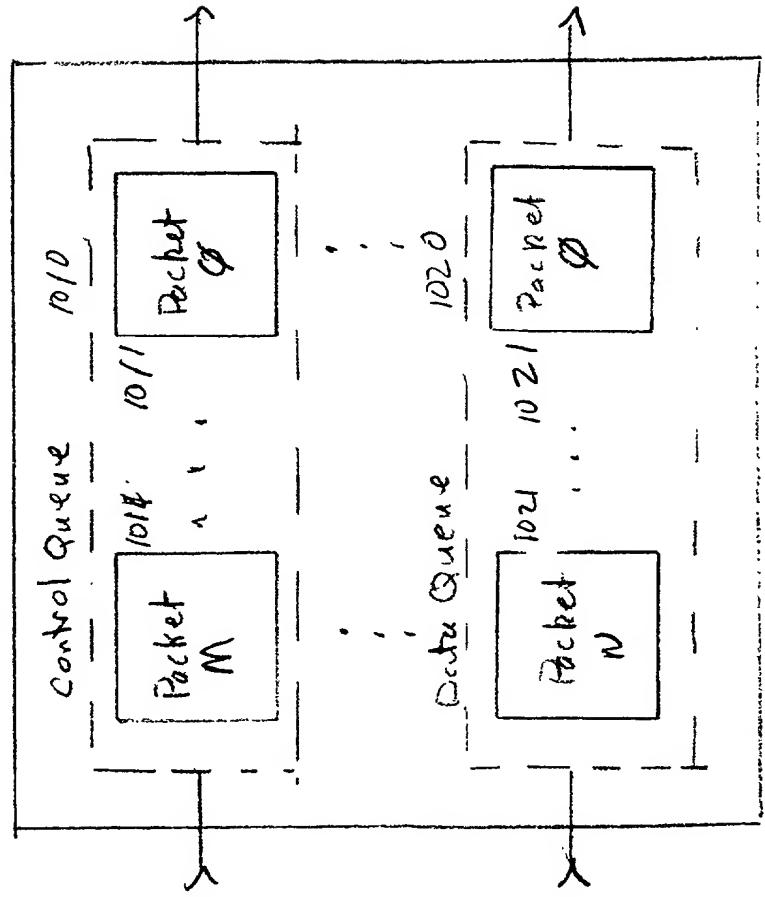


Fig 10

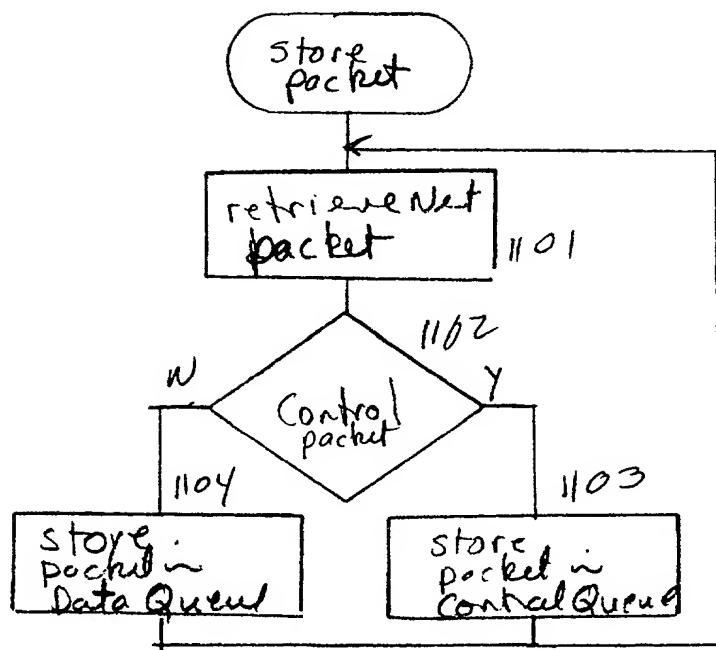


Fig 11

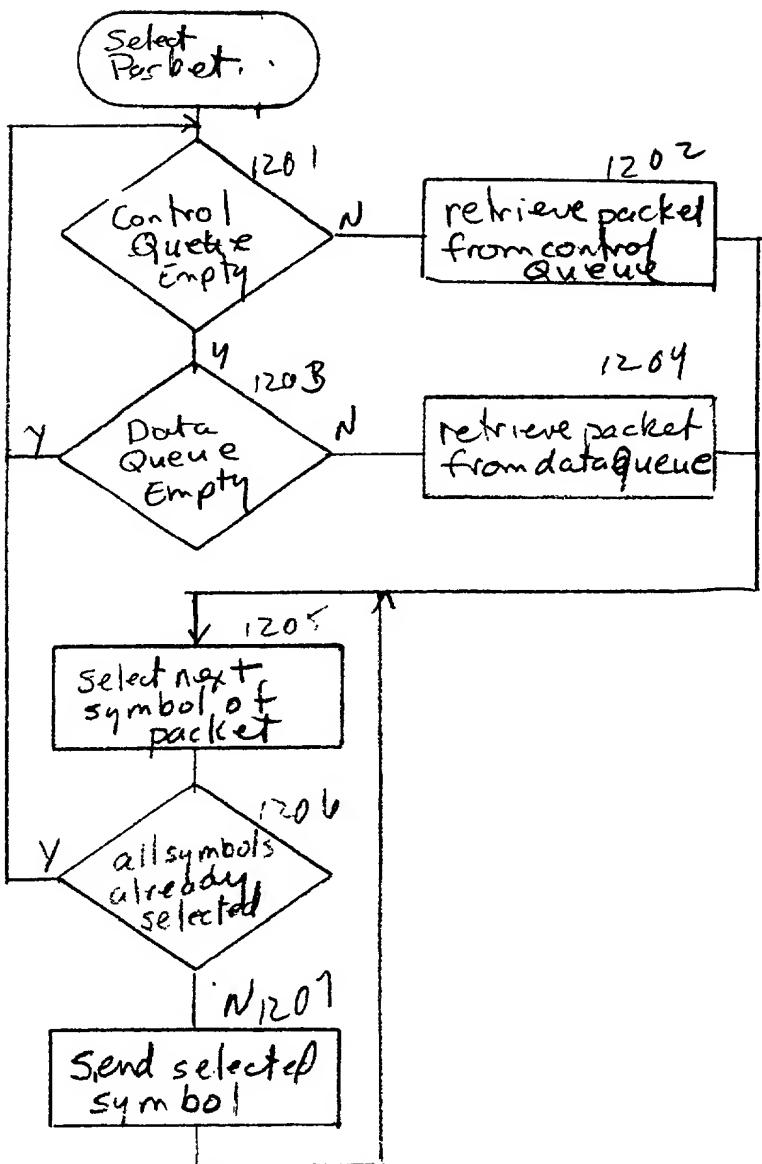


Fig 12

# TIME SLICING IN SIMPLE SCHEDULER

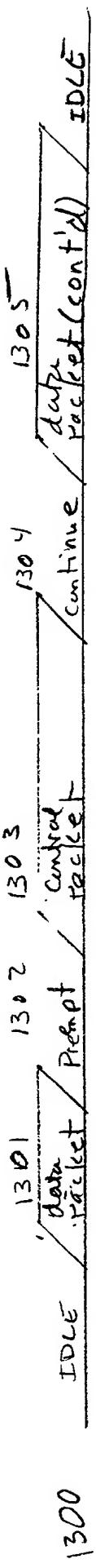


Fig 13

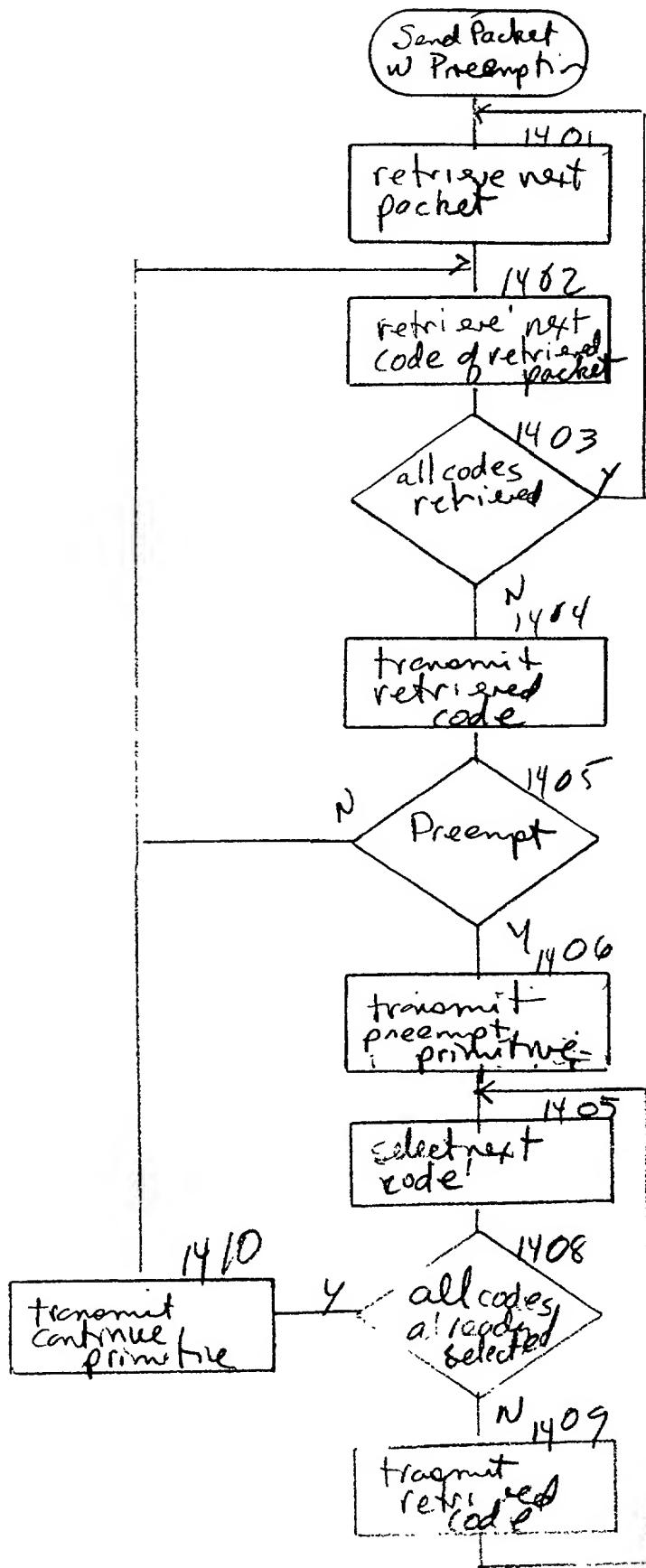


Fig 14

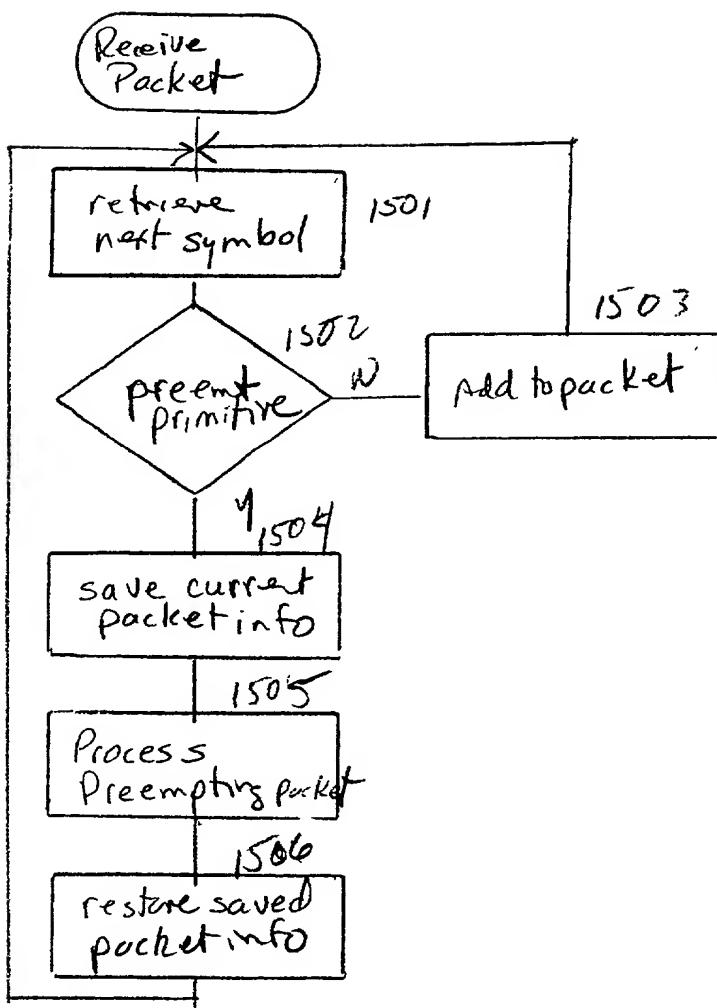


Fig 15

TOP LEVEL TESTBED

**Switch Network**

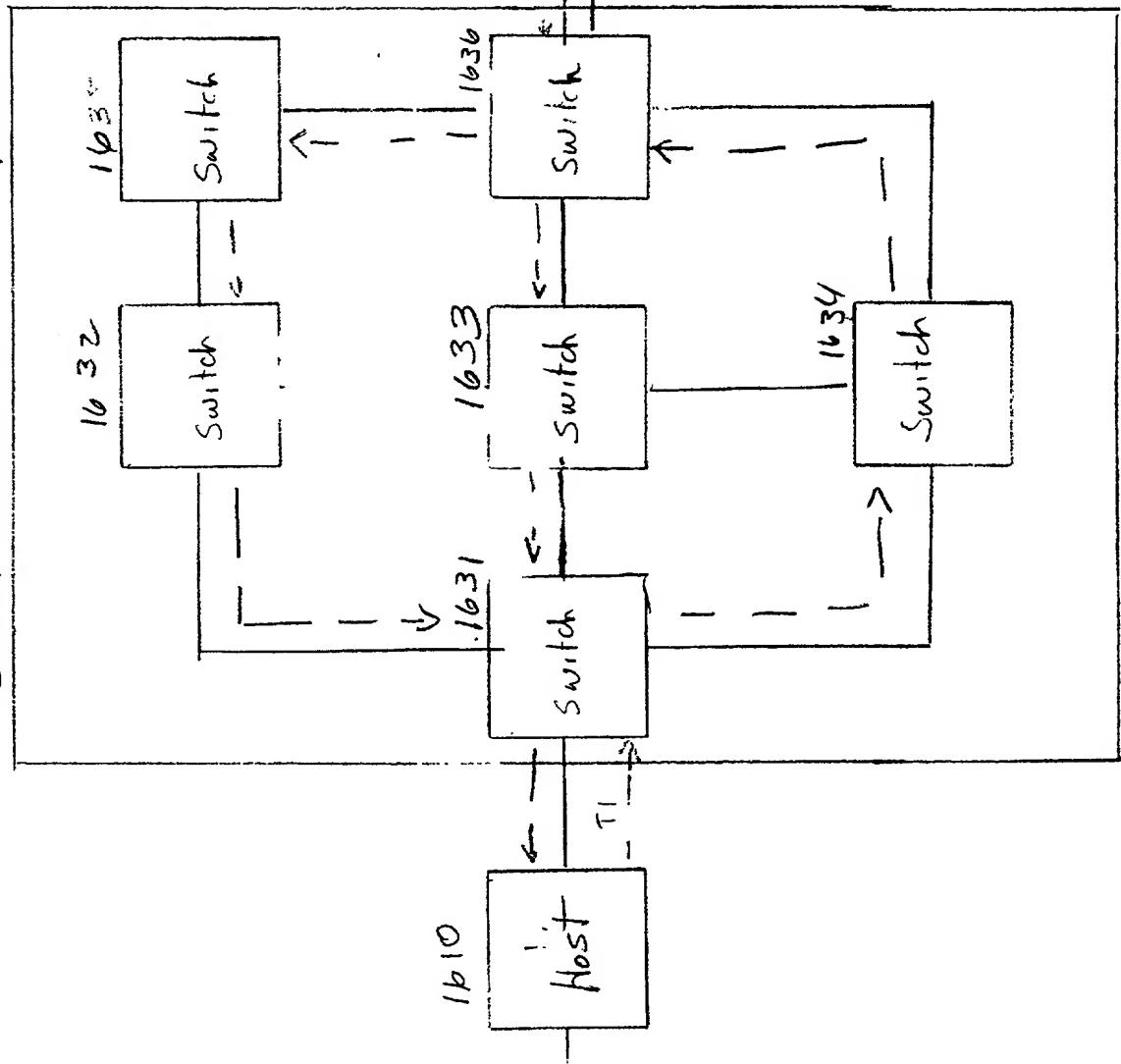
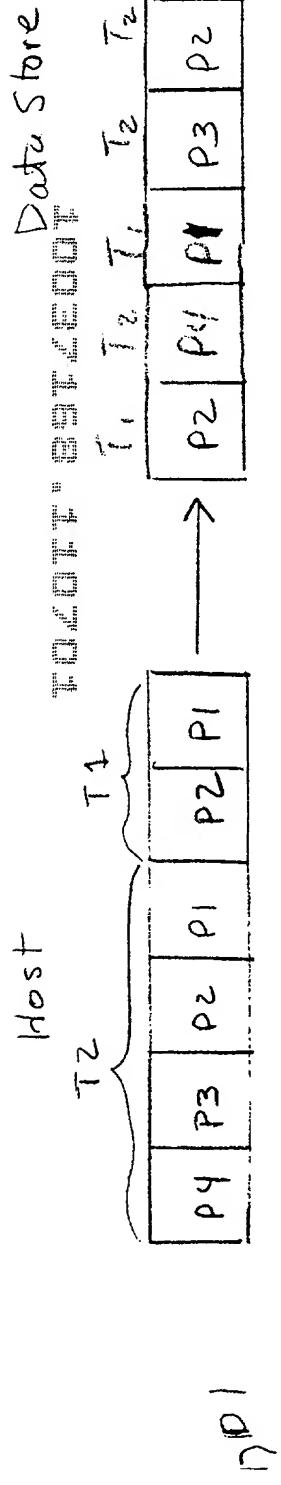
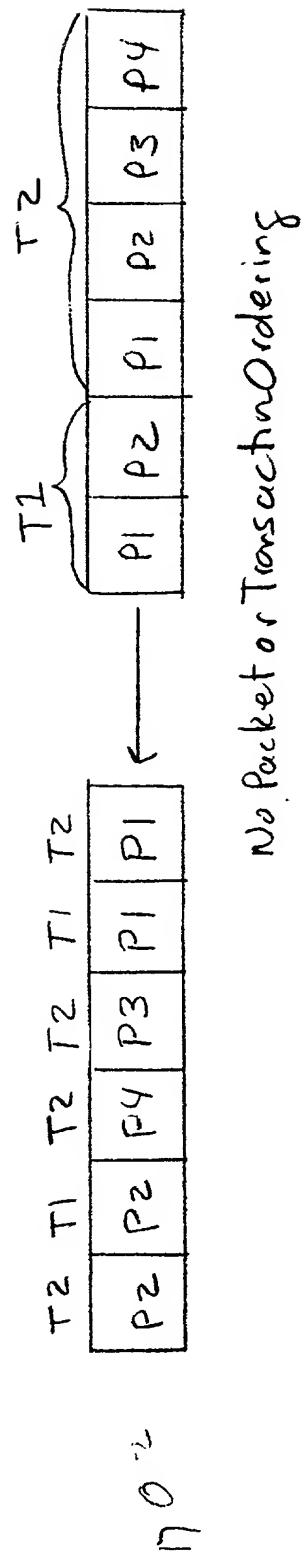


Fig 16



Preserving Packet Order w/ Transaction



No Packet or Transaction Ordering

Fig 17

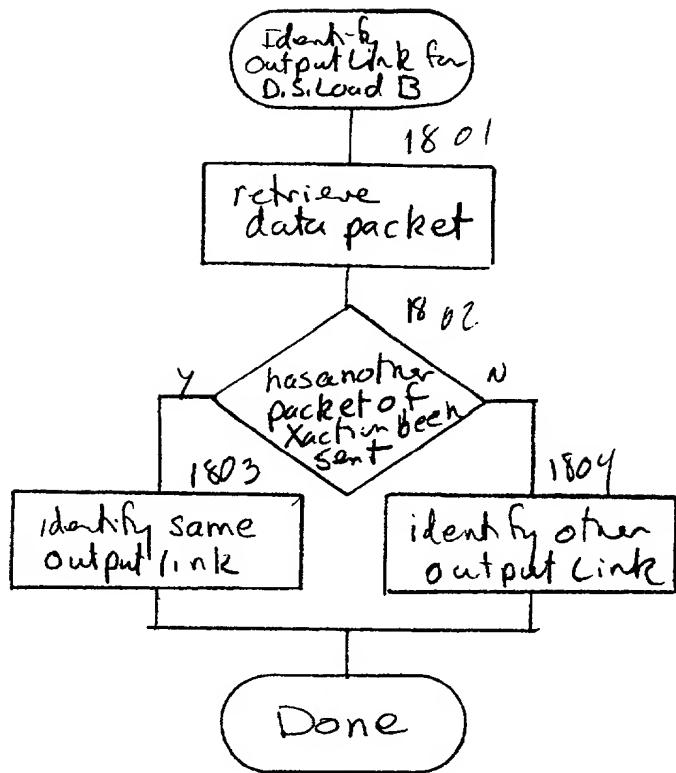
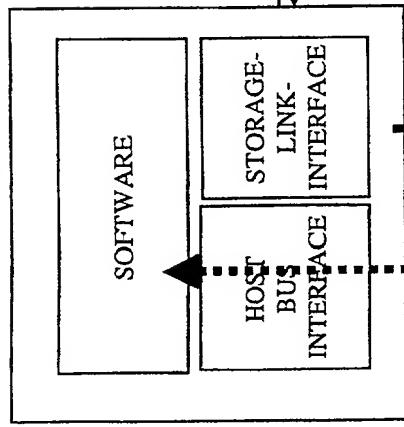
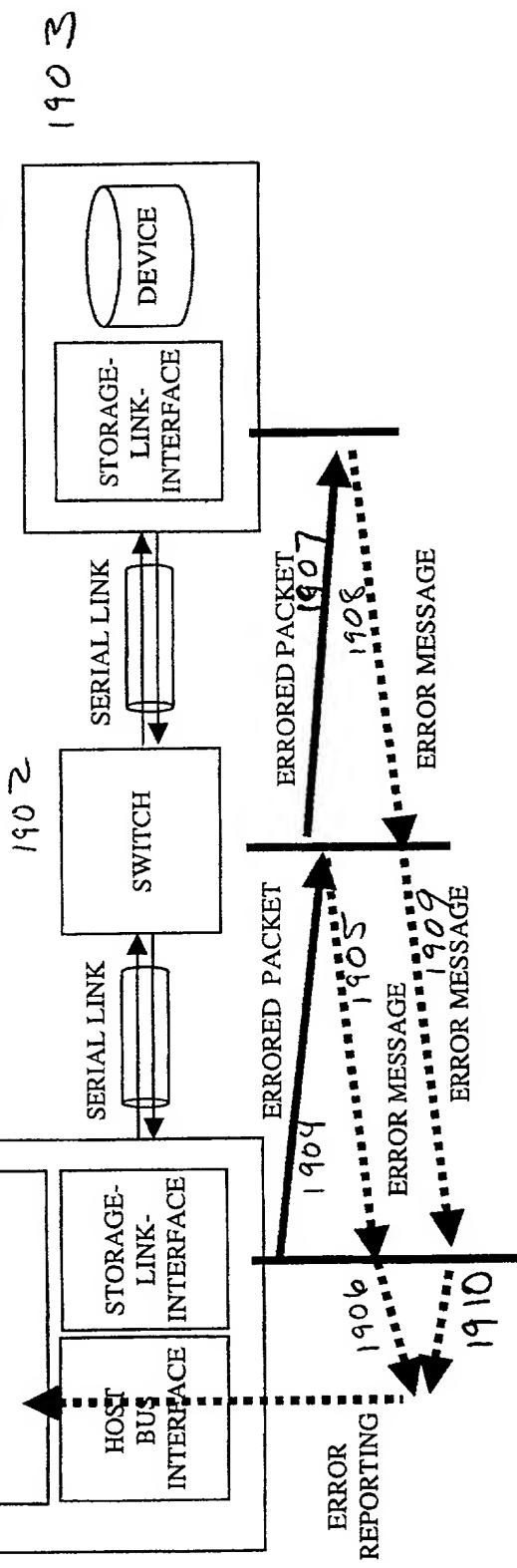


Fig 18

Host 1901



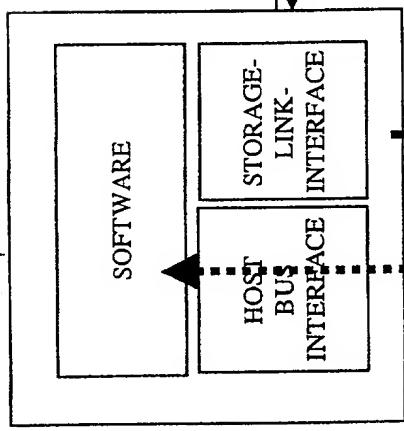
Data Store Device



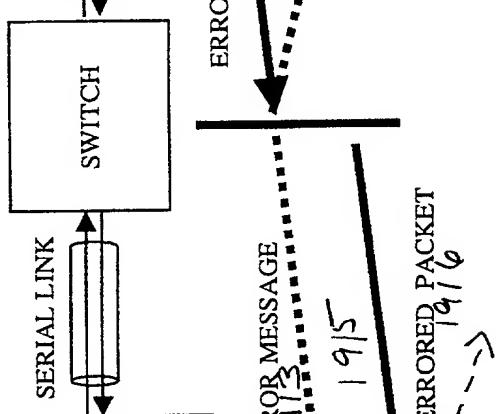
1909

Fig 19 A

host 1901



1902



Data Shredder

1903

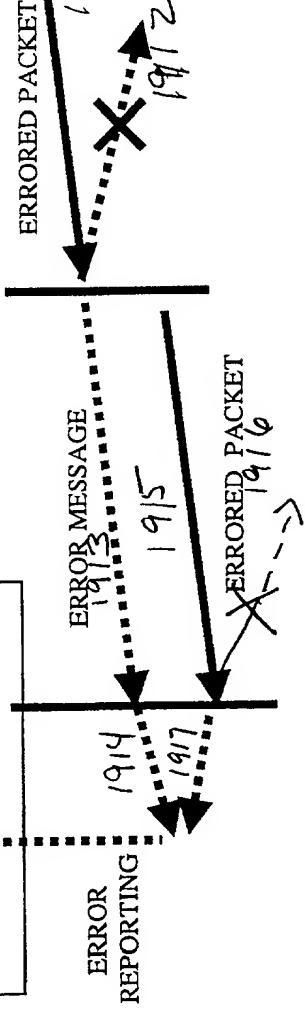
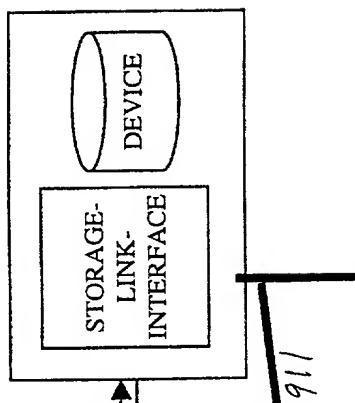
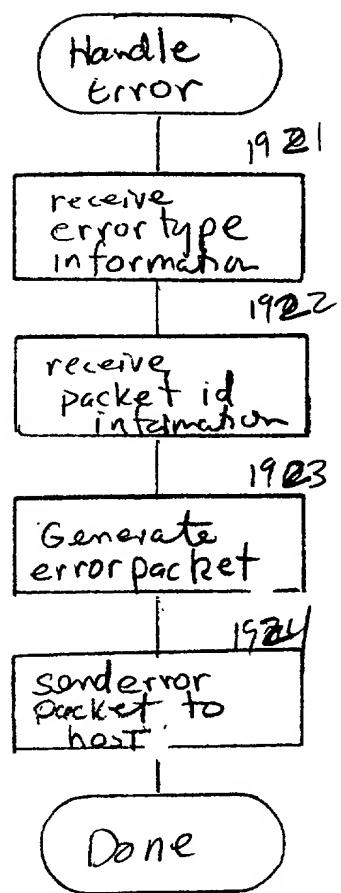


Fig 18 19B

1900



19C

8 b code	9 bit symbol
0000 0000	101010101
0000 0001	101010100
0000 0010	101010111
:	
0101 0101	001010101
:	
0111 0110	001110110
0111 0111	100100010
:	
1111 1111	110101010

Fig 20

FILED BY T. E. COOPER

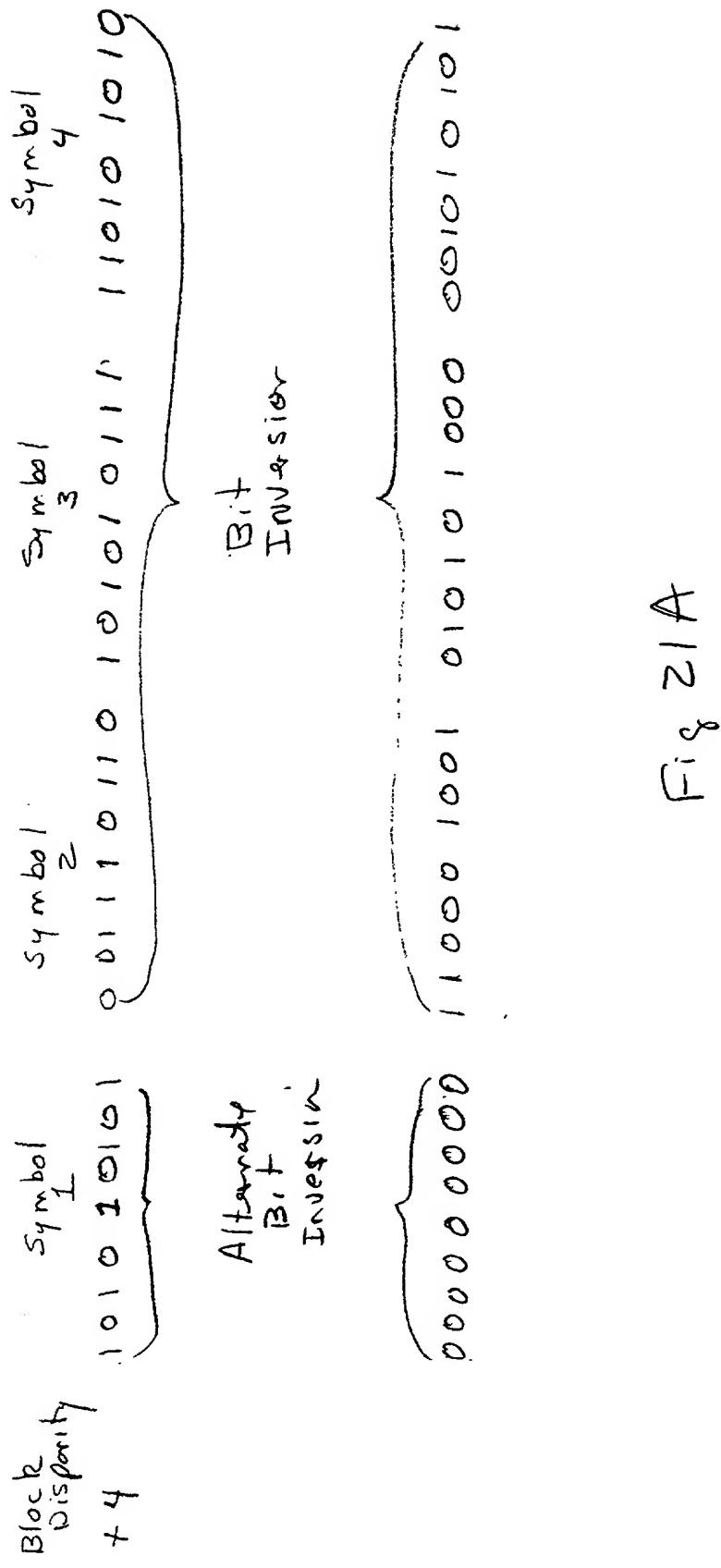


Fig 21A

TIME FLOW

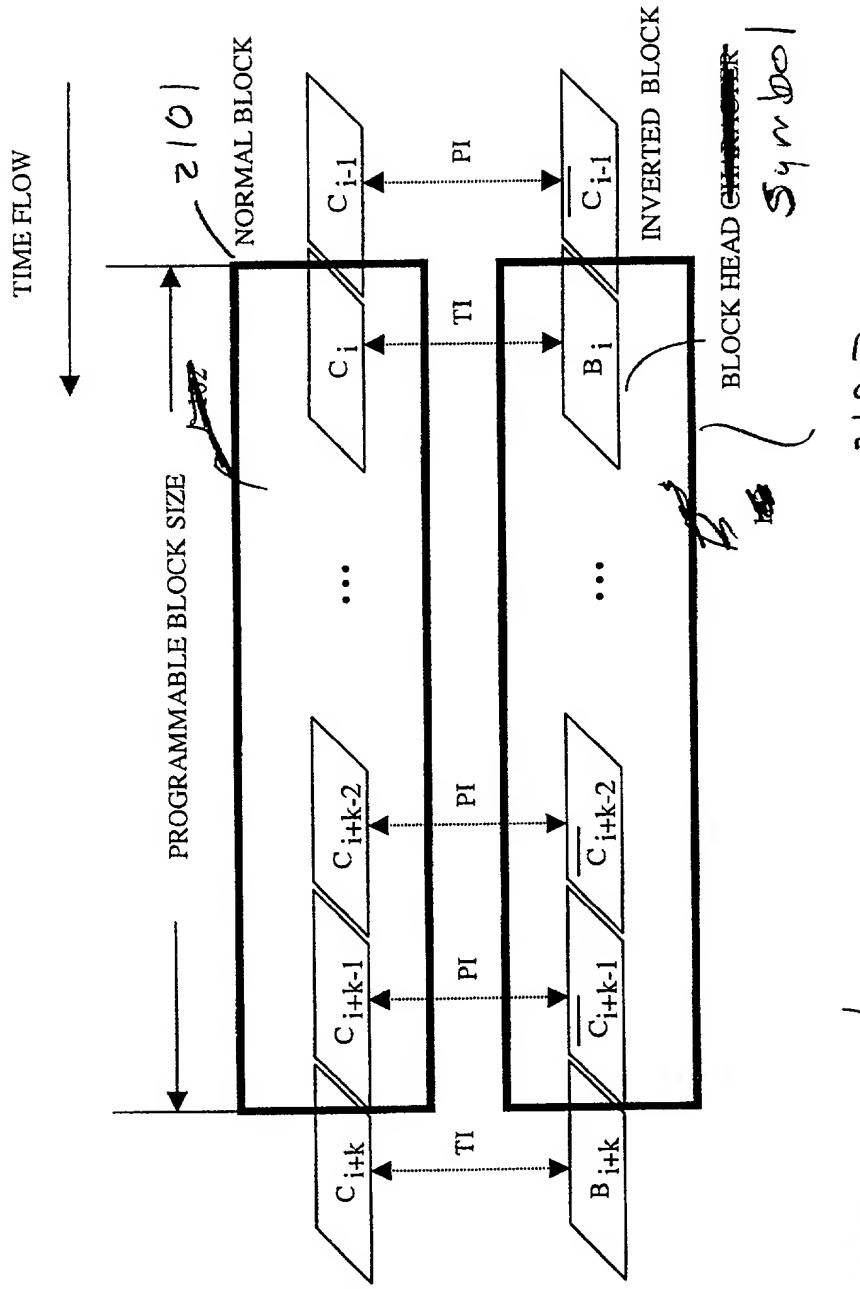
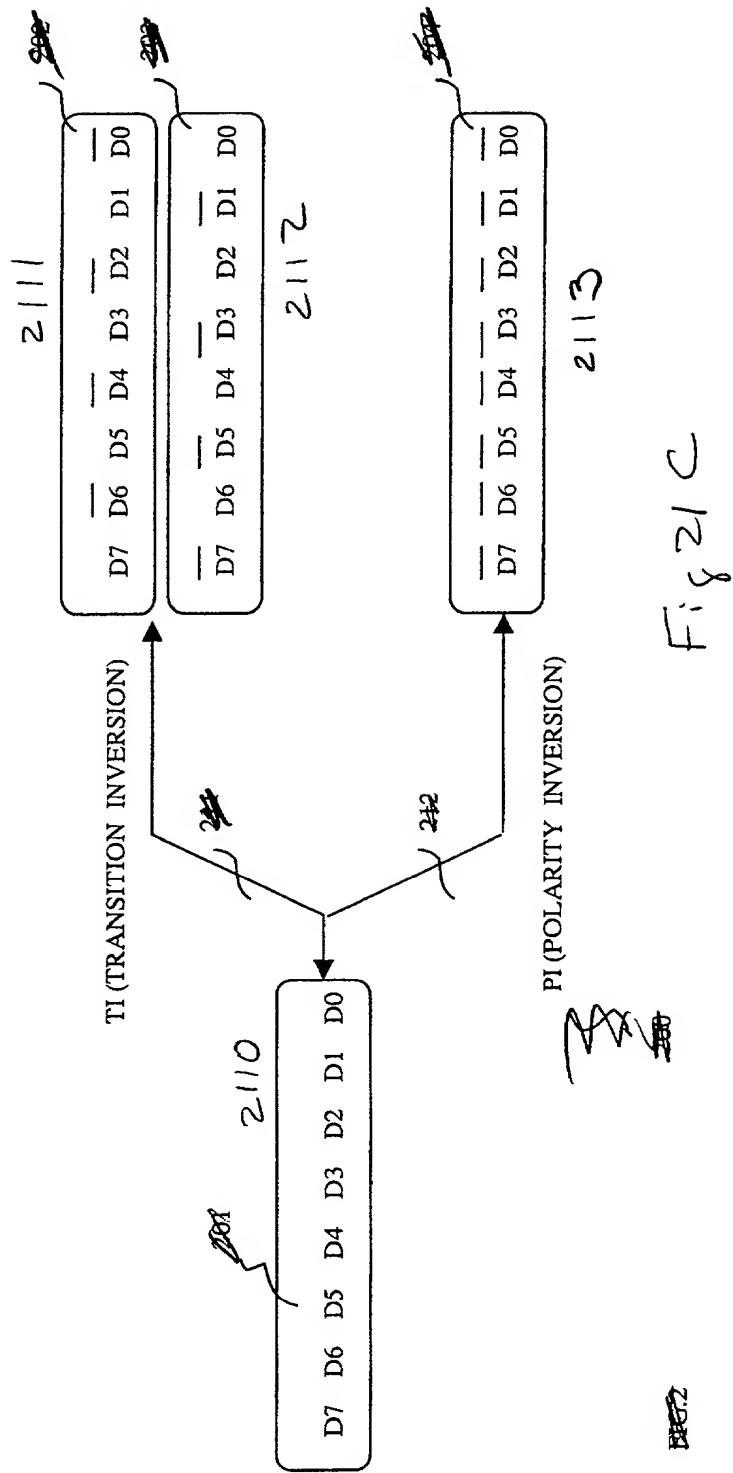


Fig 21 B

2110 2111 2112 2113



2112

Fig 21C

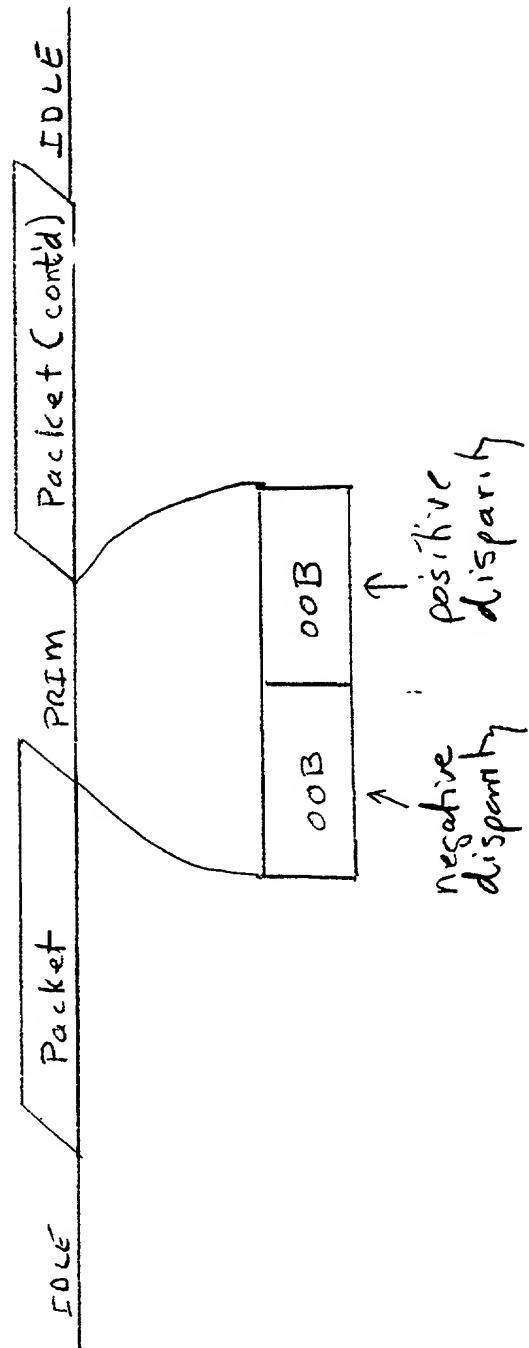


Fig 22

0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

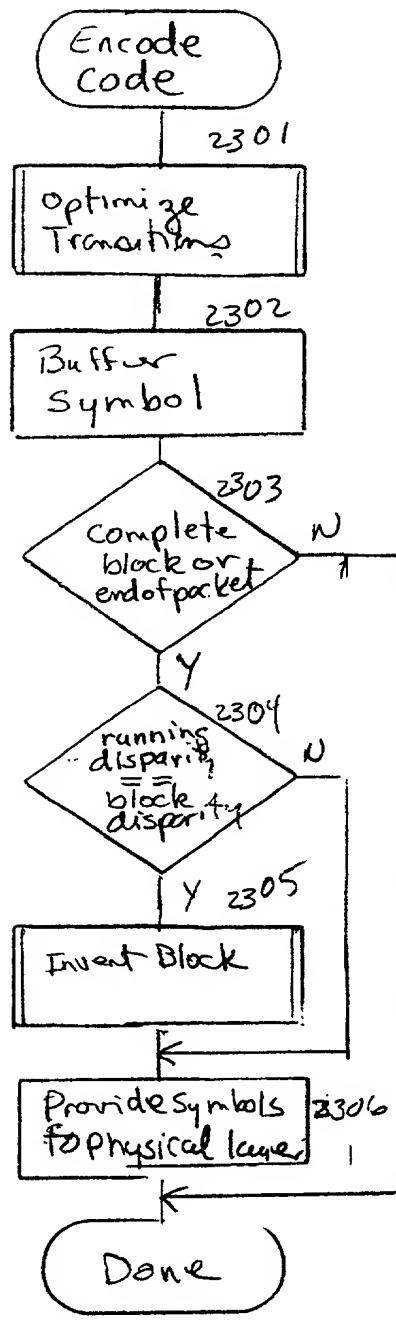


Fig 23

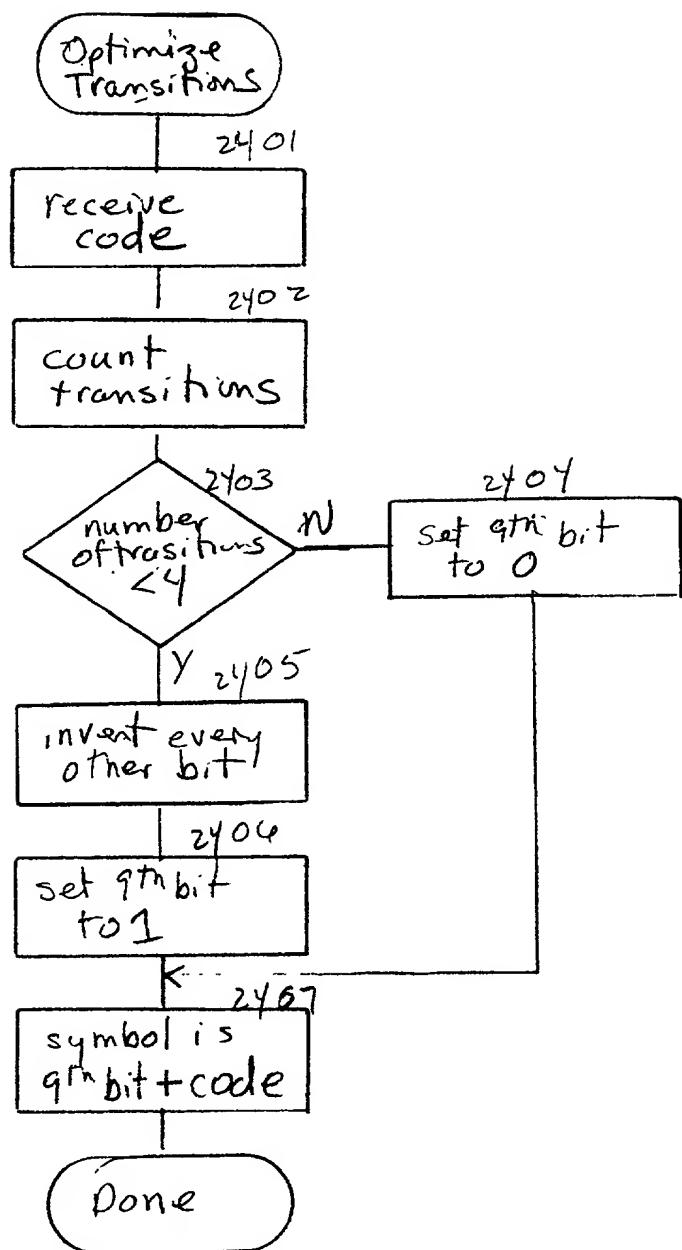


Fig 24

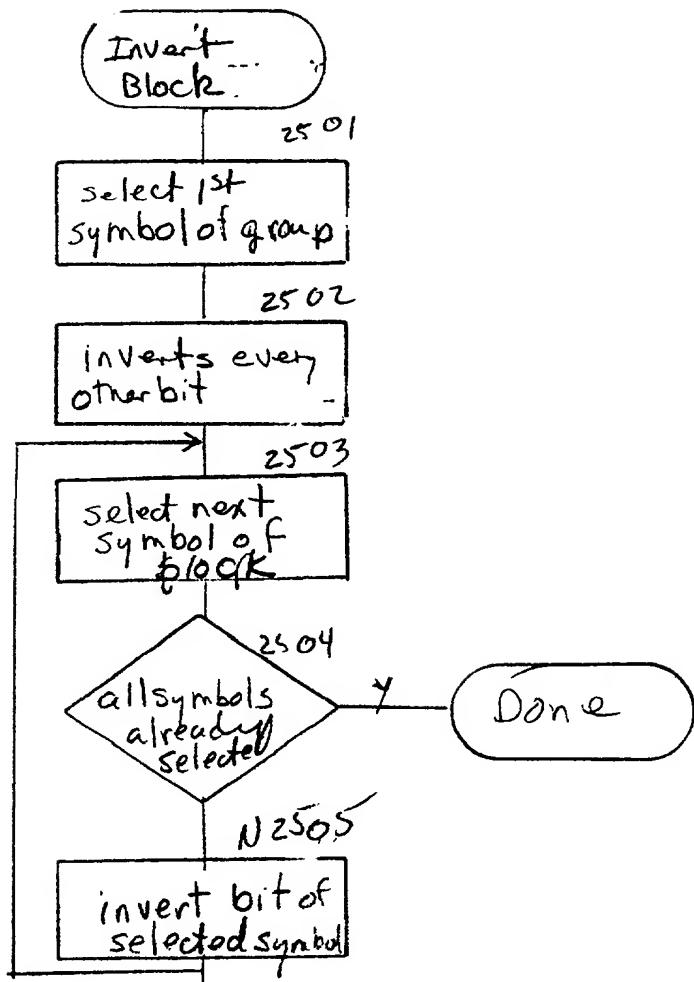


Fig 25—

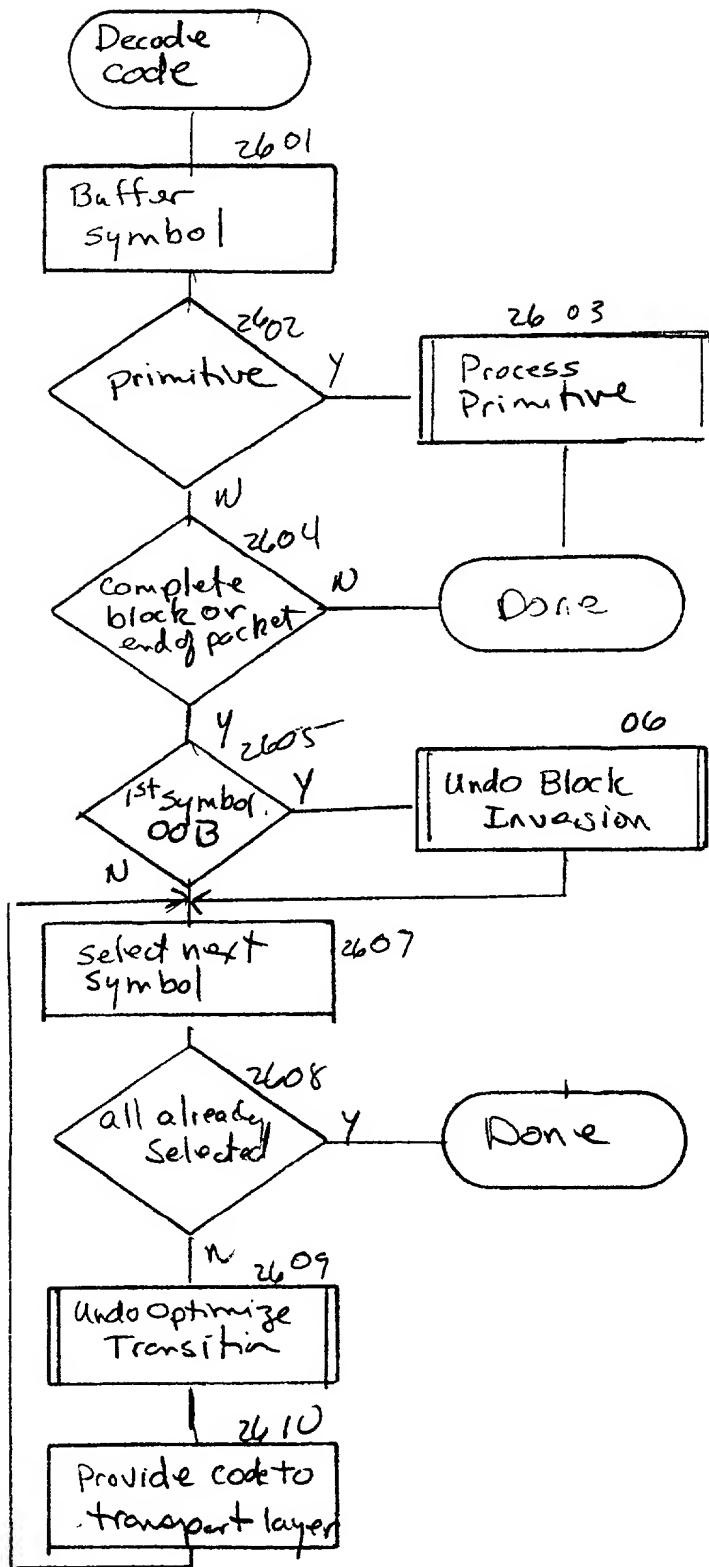


Fig 26

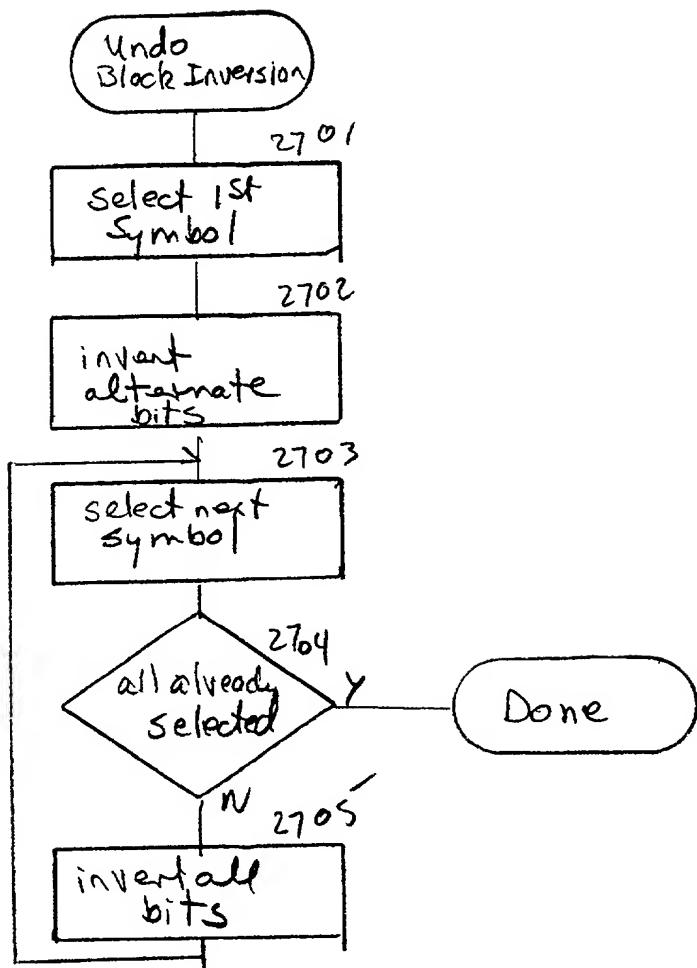


Fig 27

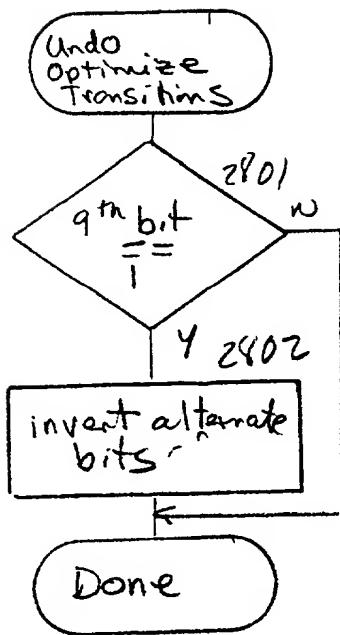


Fig 28

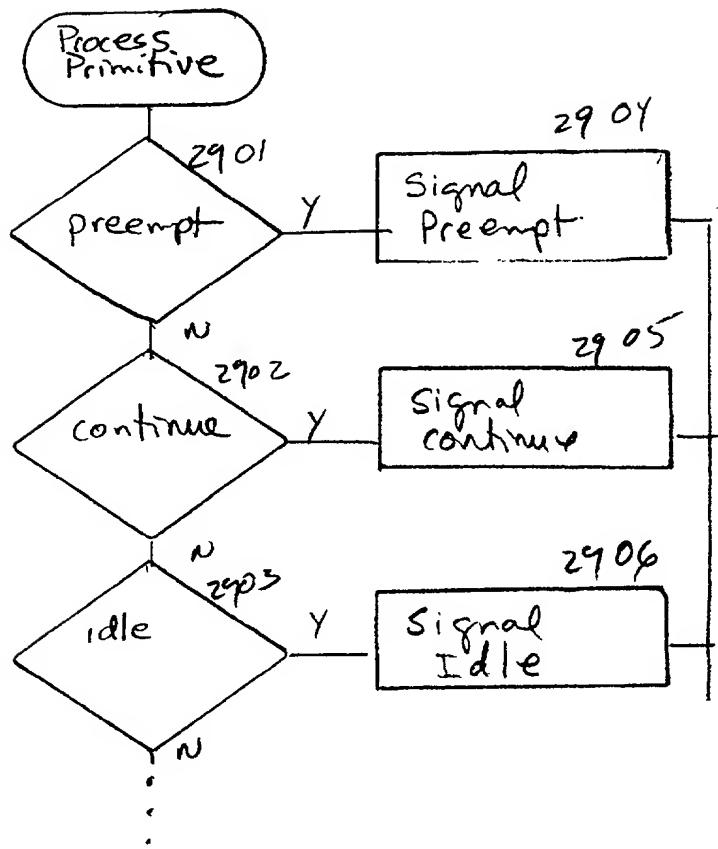


Fig 29

## Multipoint Memory Dance

30.00

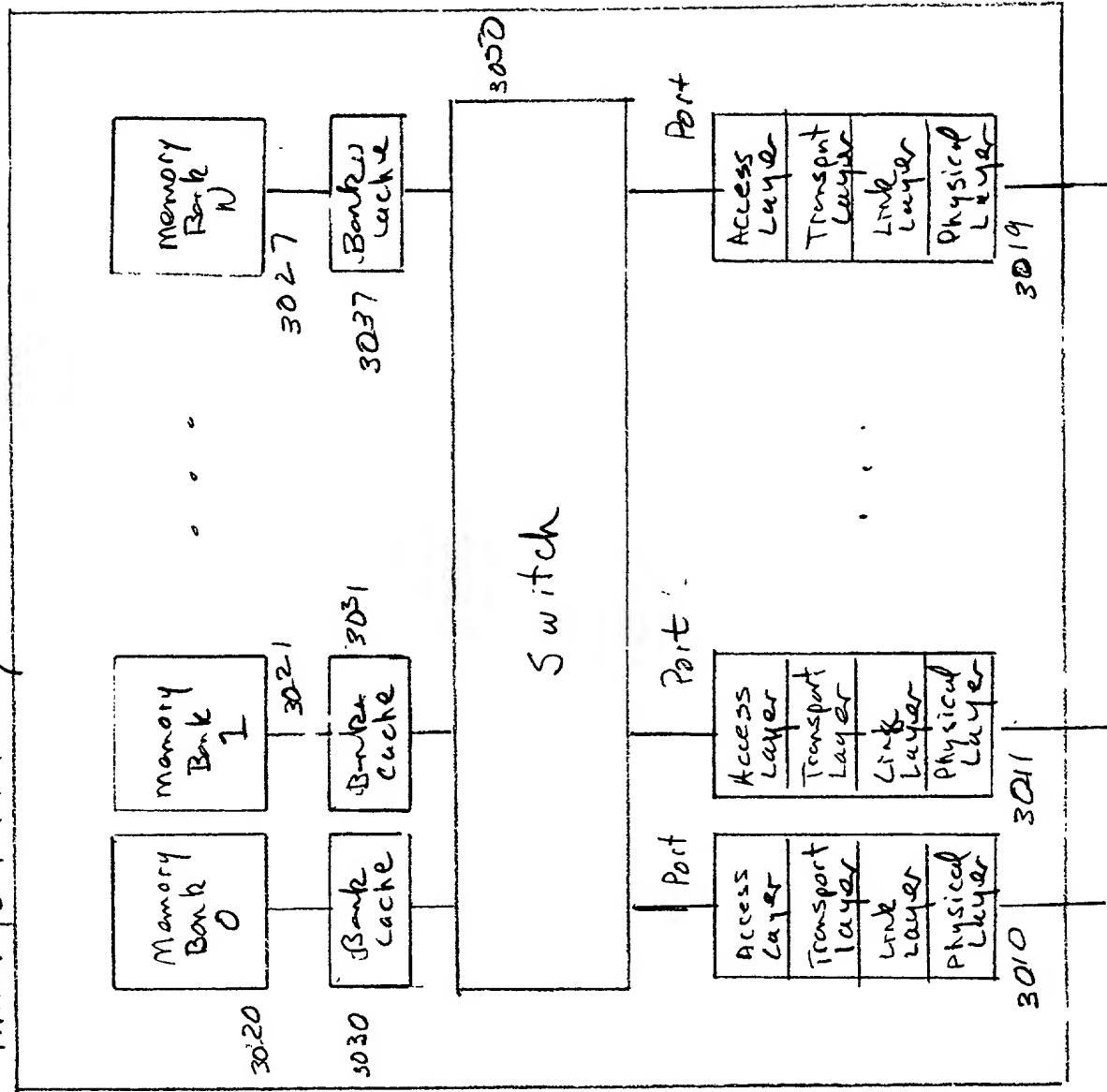
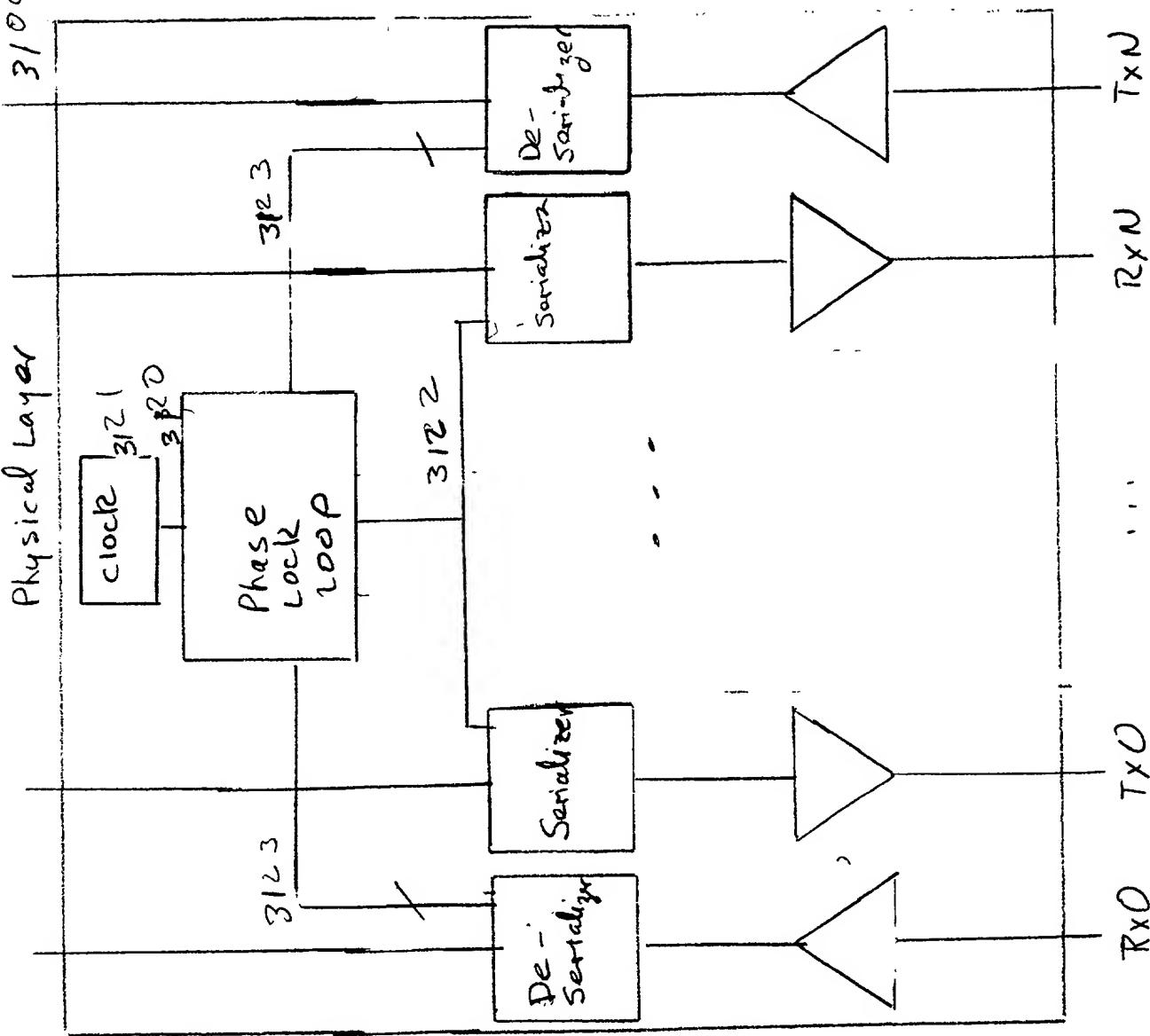


Fig 30

3100

Physical Layer



3110

Fig 3.1

3119

RxN

TxO

TxN

Port	Input Queue 3201		
	R/W	Address	Data
3	R	1000	
4	W	4000	10...1
3	W	1000	111..0
3	R	2000	

Port	Output Queue 3202		
	Valid	Port	Data
1	3		11...0
	0		
	0		
1	3		101...1

Fig 32

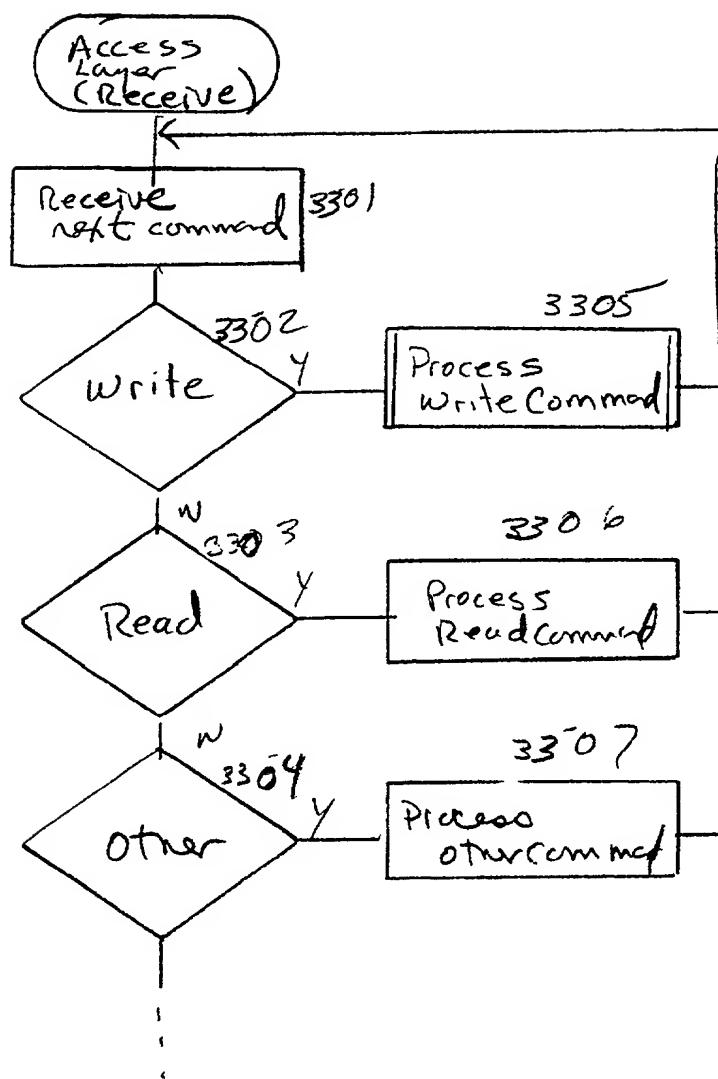


Fig 33

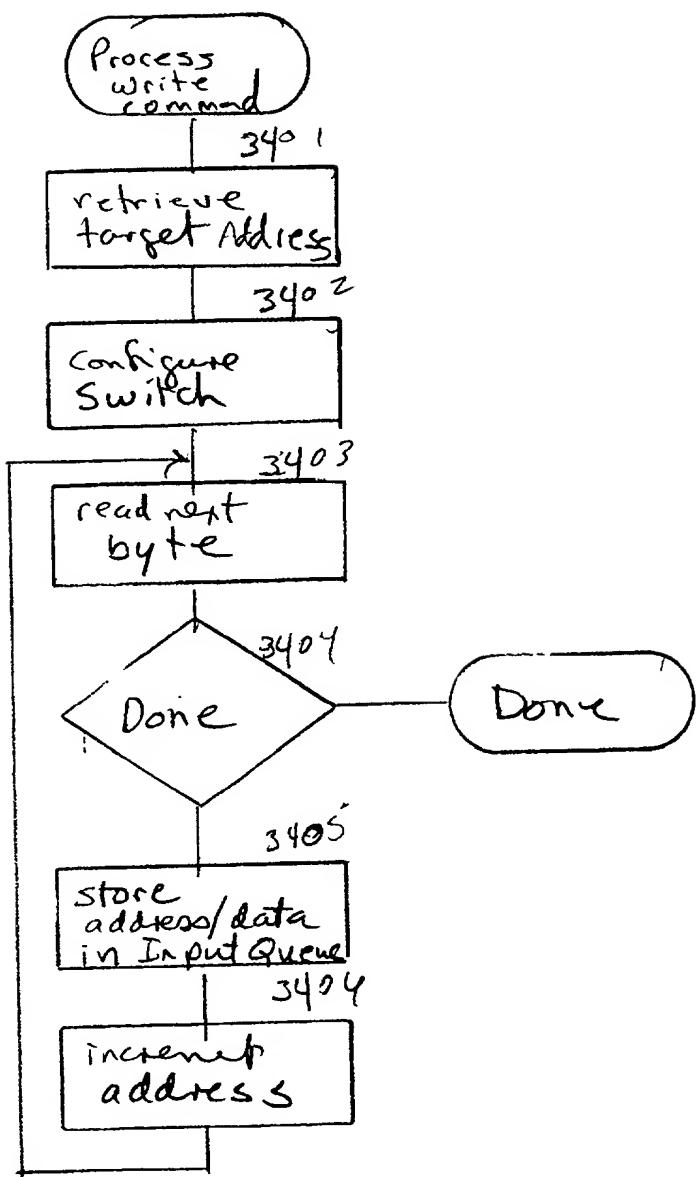


Fig 34

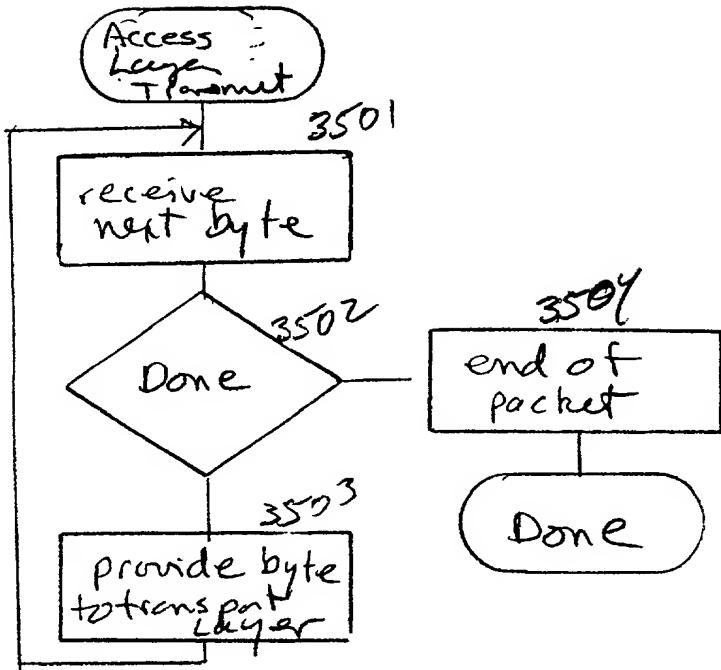
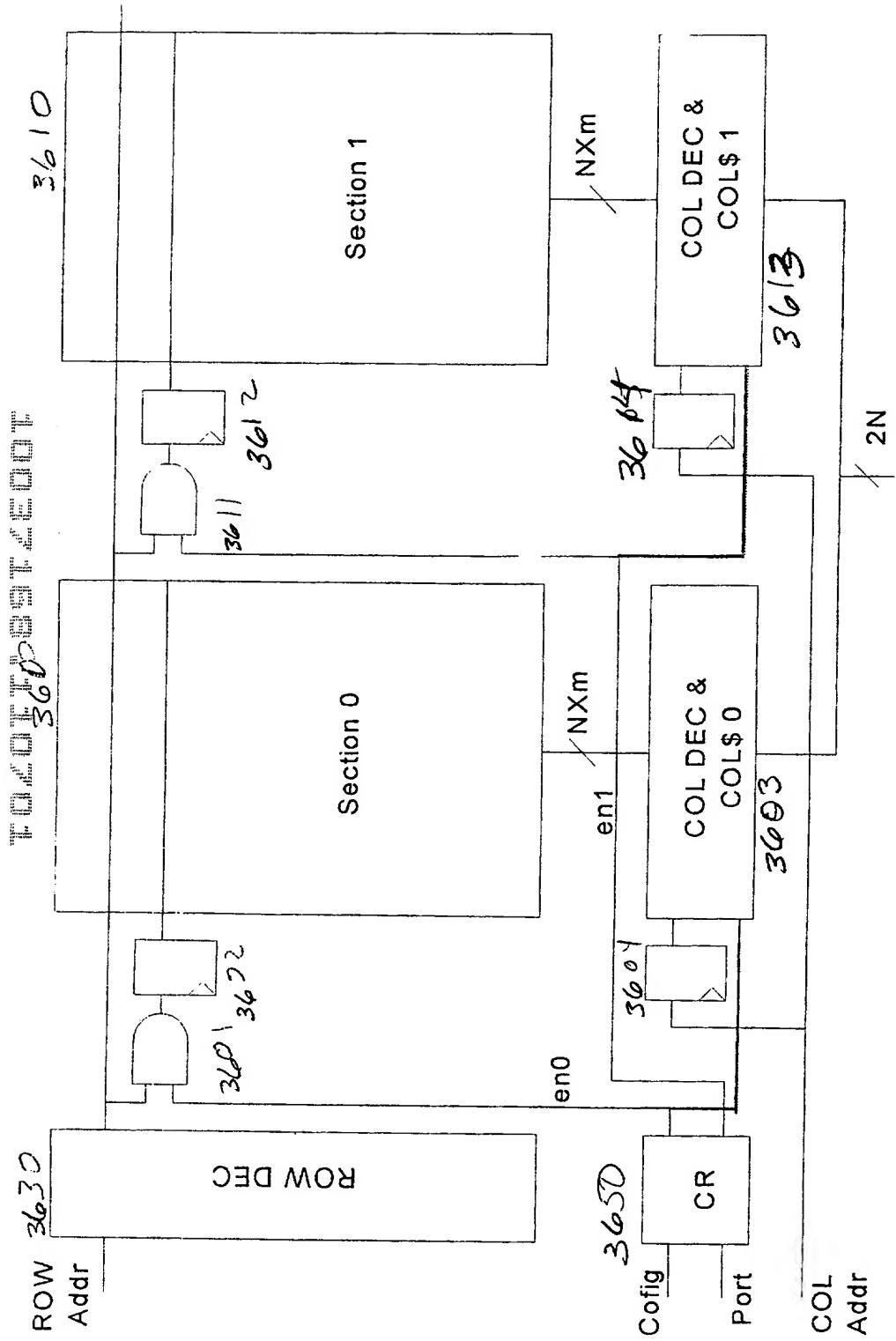
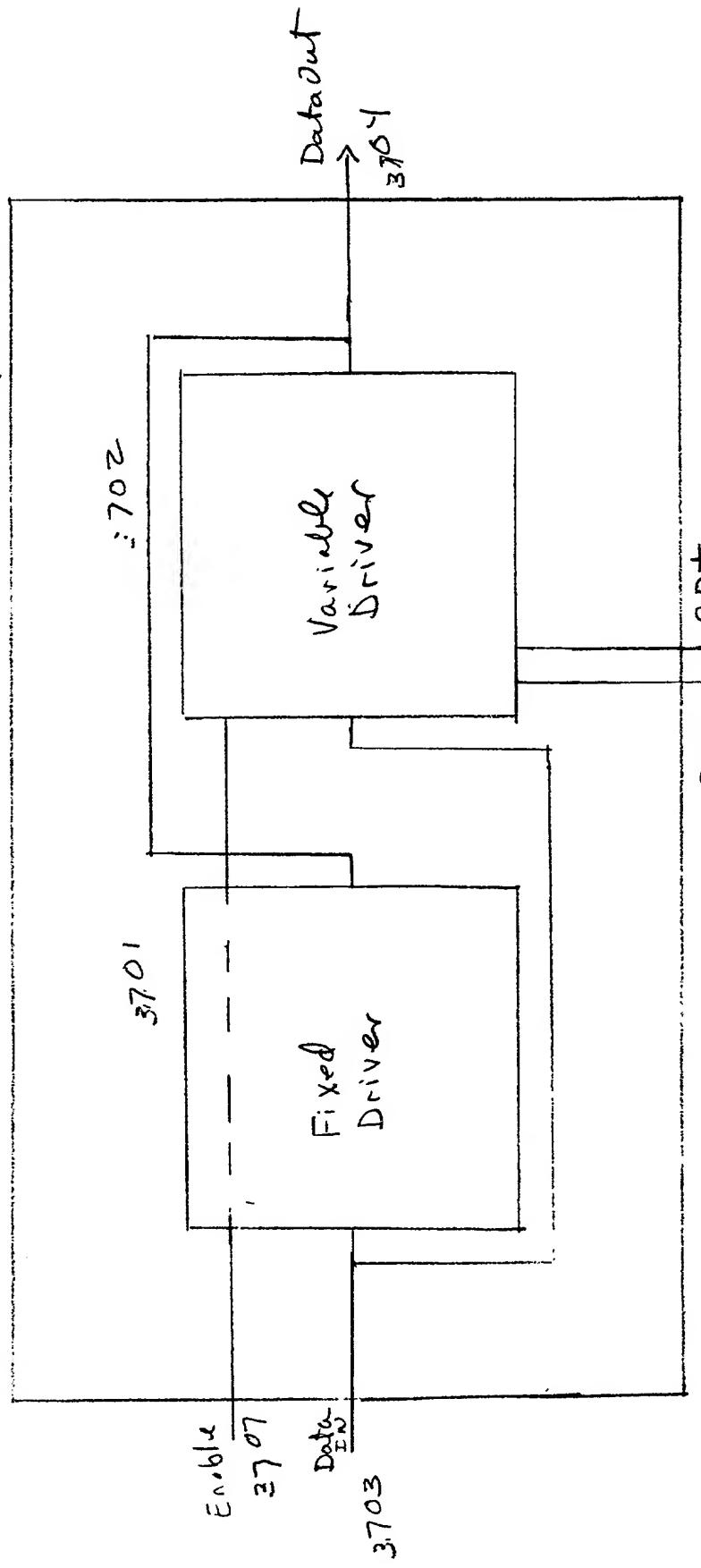


Fig 35



Line Driver 3700



$$\begin{cases} RD^+ \wedge \overline{Data_{Io}} = pull\ down \\ RD^- \wedge Data_{In} = pull\ up \end{cases}$$

## Variable Drivers

Fig 37A

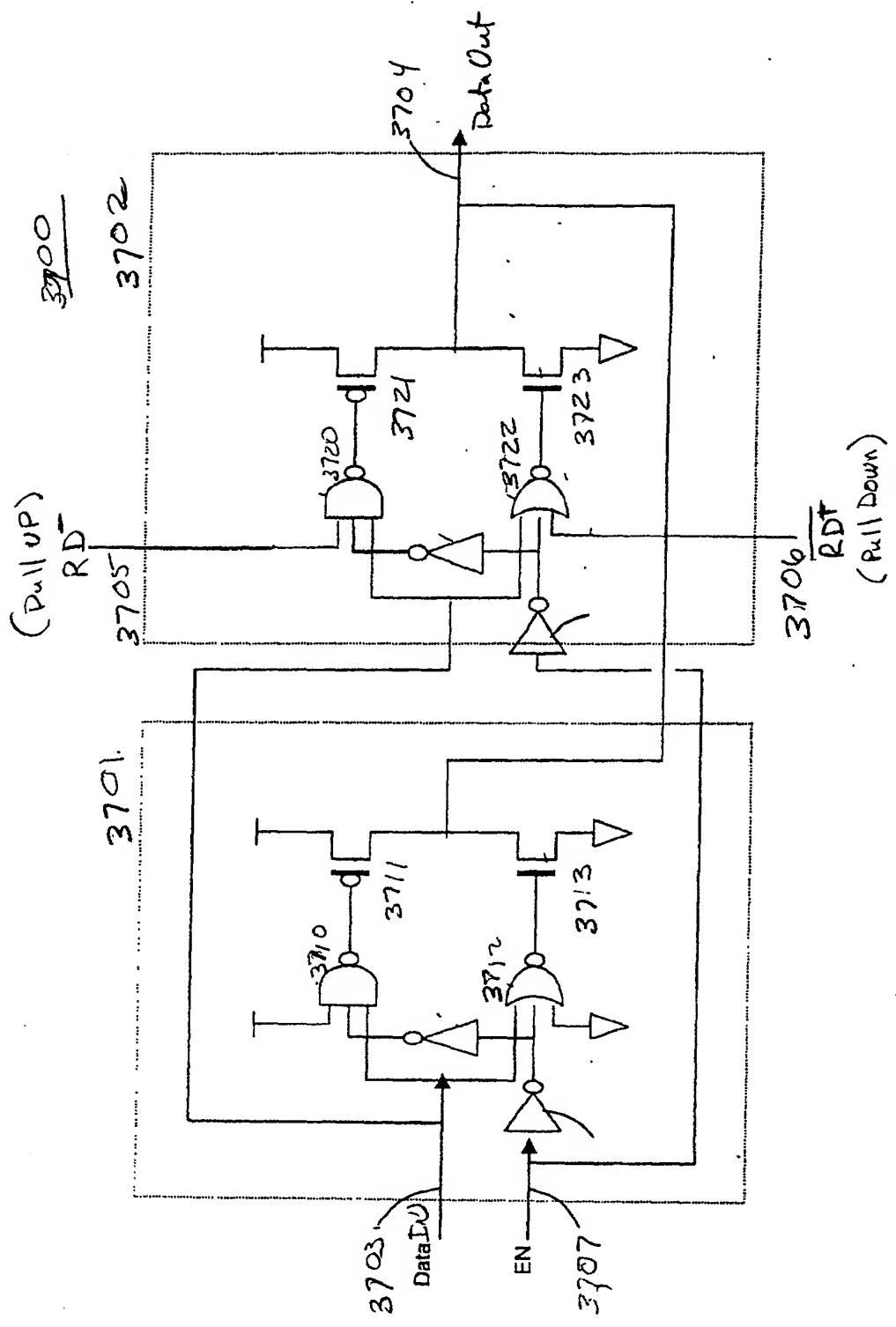


Fig 3713

# FIGURE 38.10 Fast Ethernet

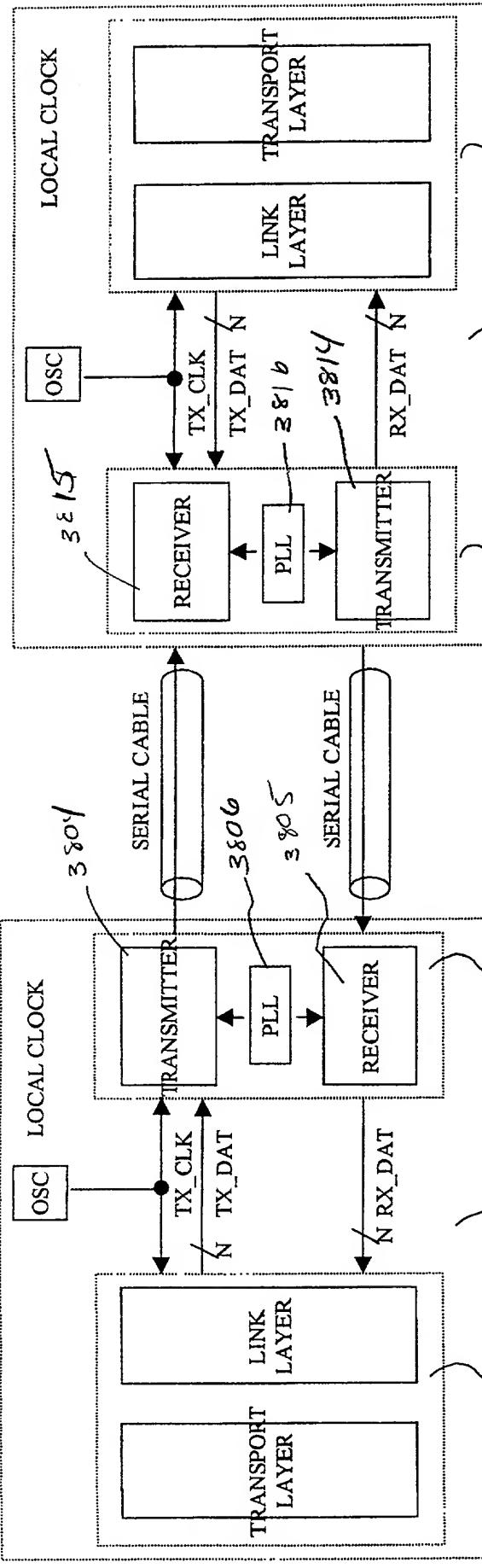


Fig 38A

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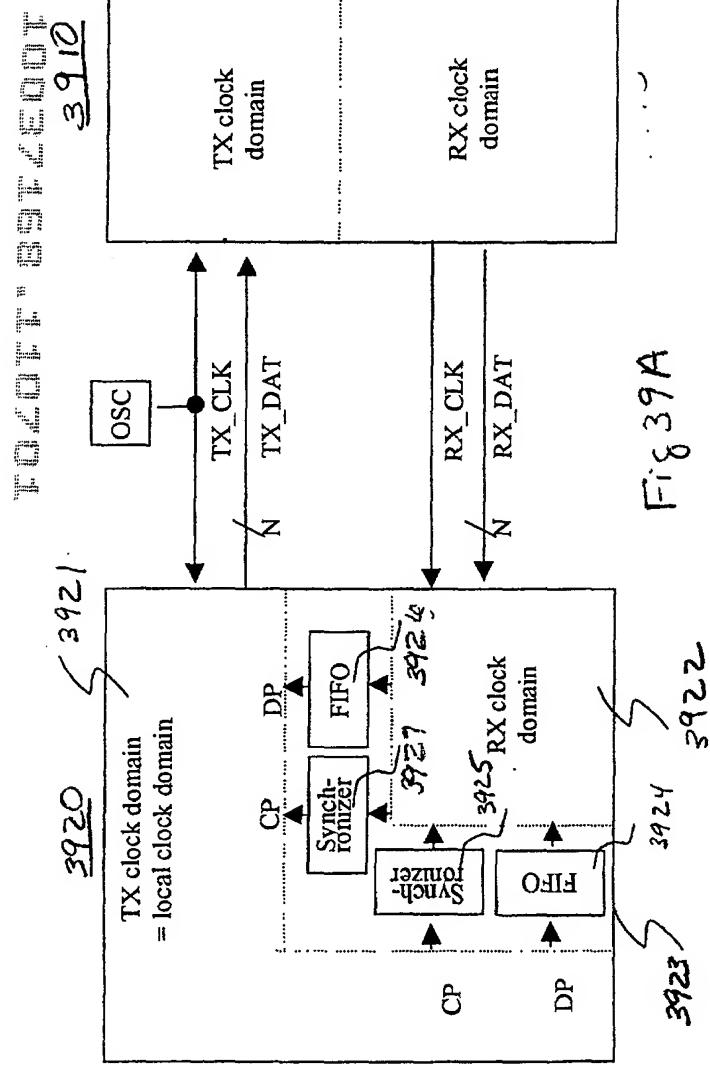


Fig 39A

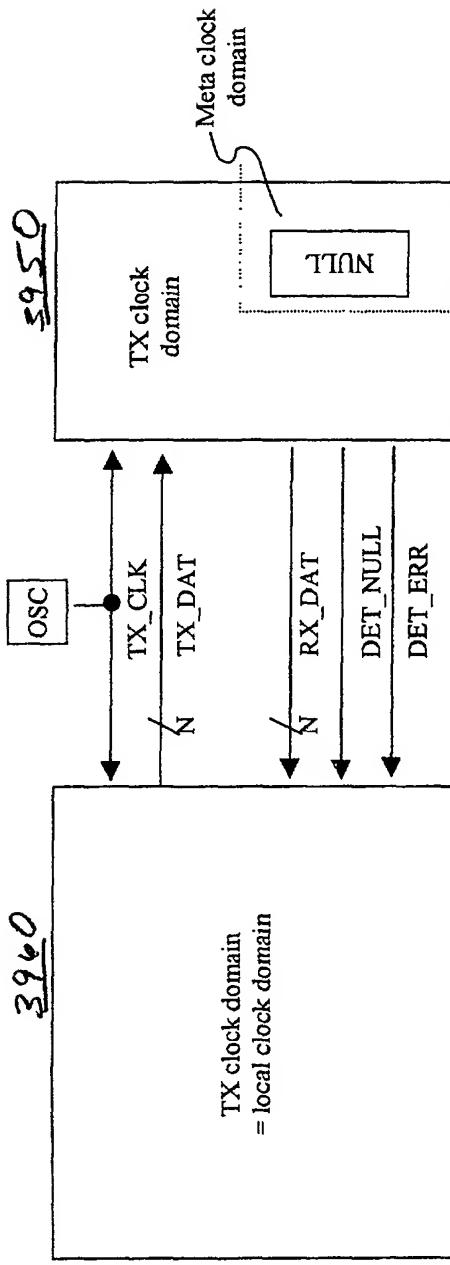


Fig 39B

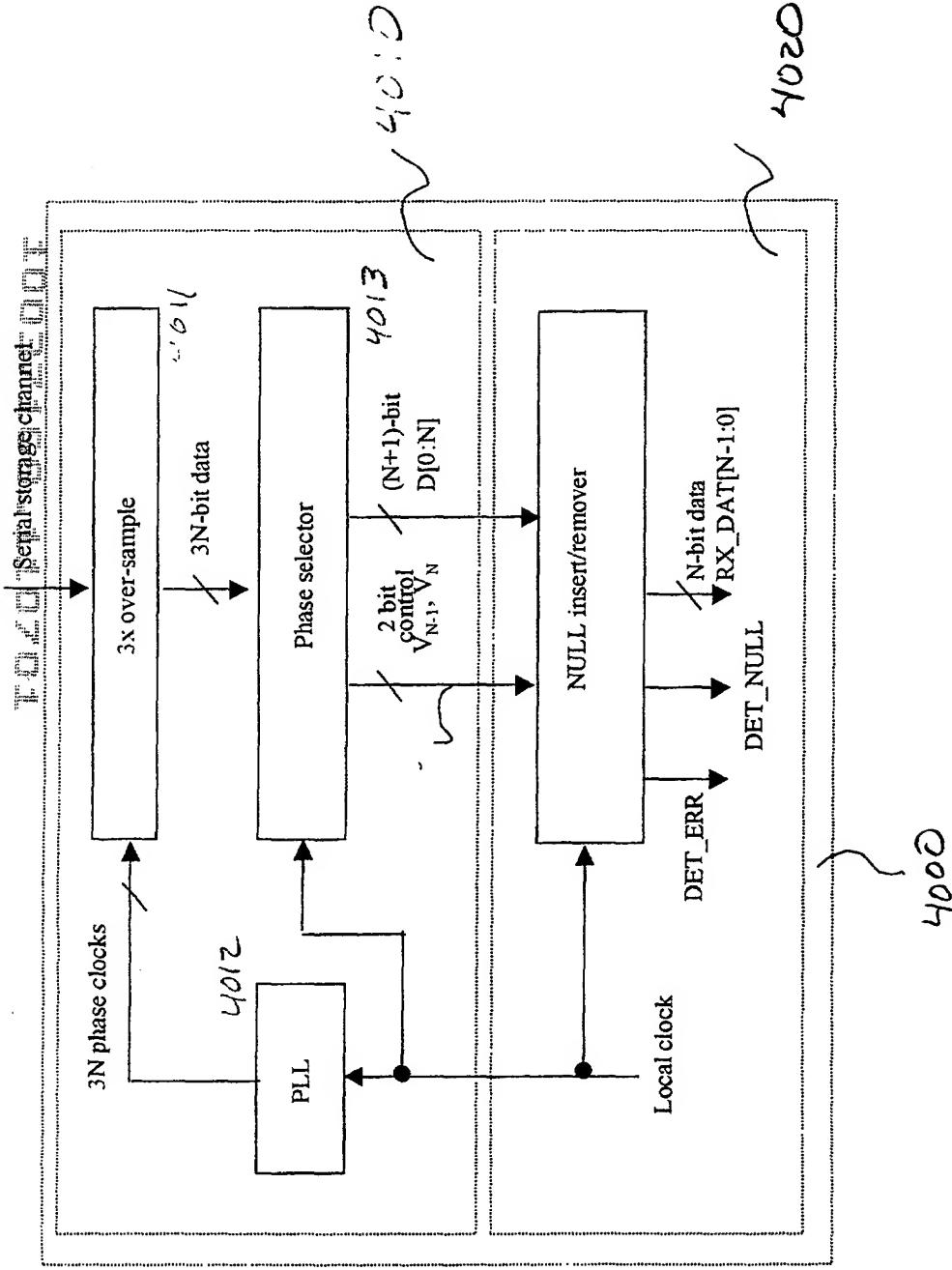


Fig 4D

LOCAL CLOCK

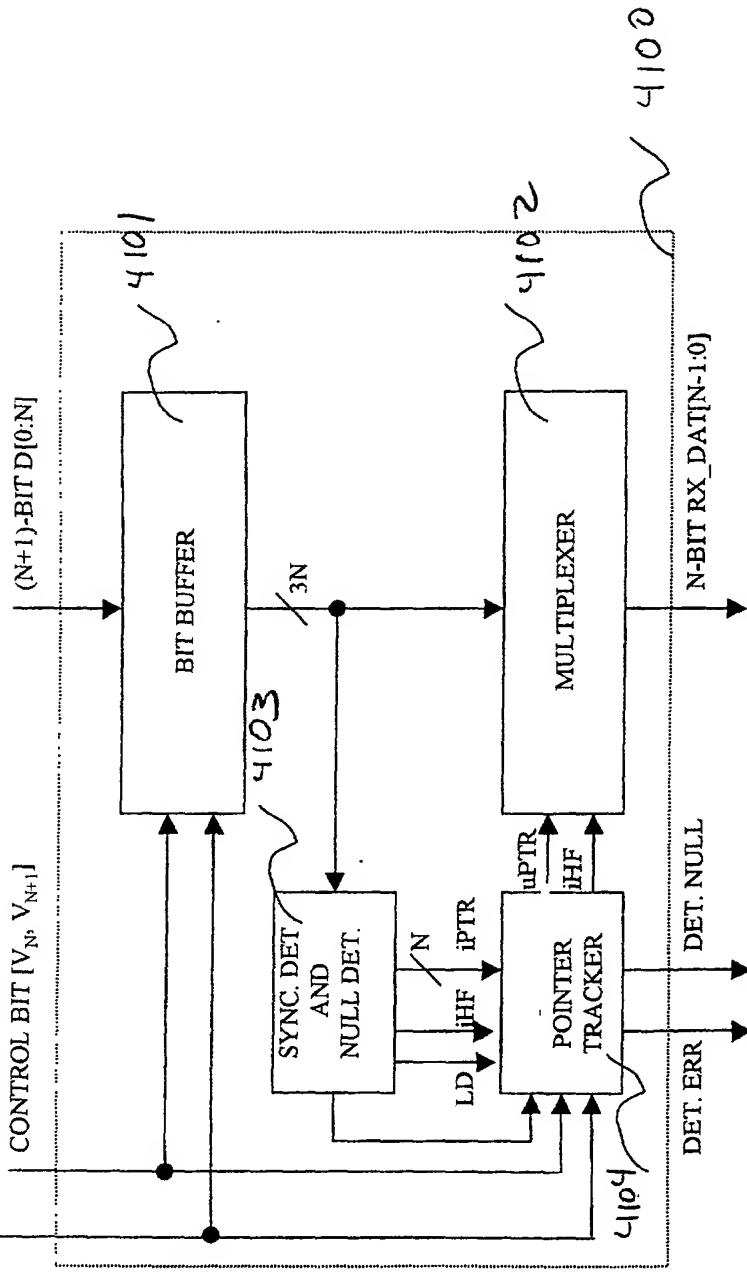


Fig 41

Figure 8.42 shows

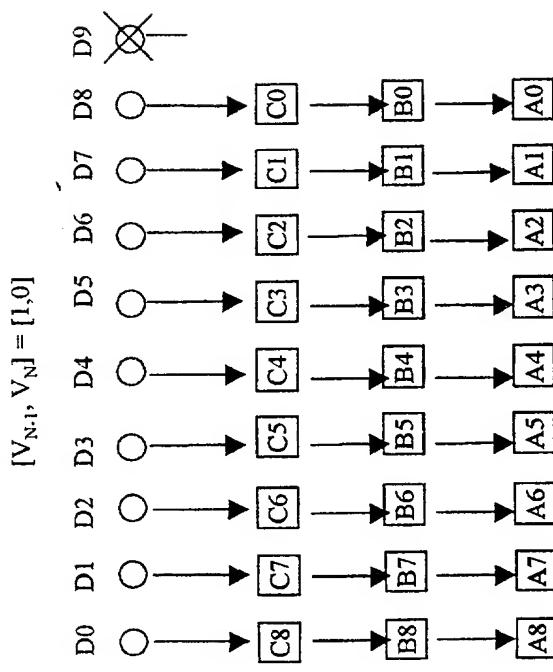


Figure 8.42

$[V_{N,1}, V_N] = [0,0]$

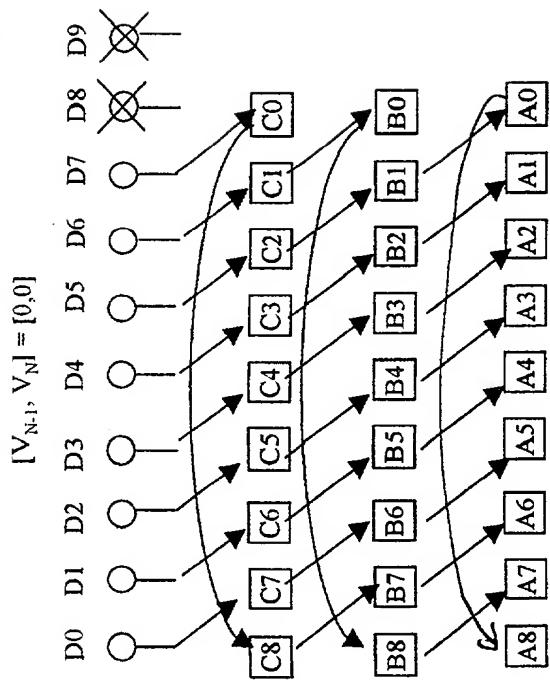


Fig 42 B

图 8.42 C

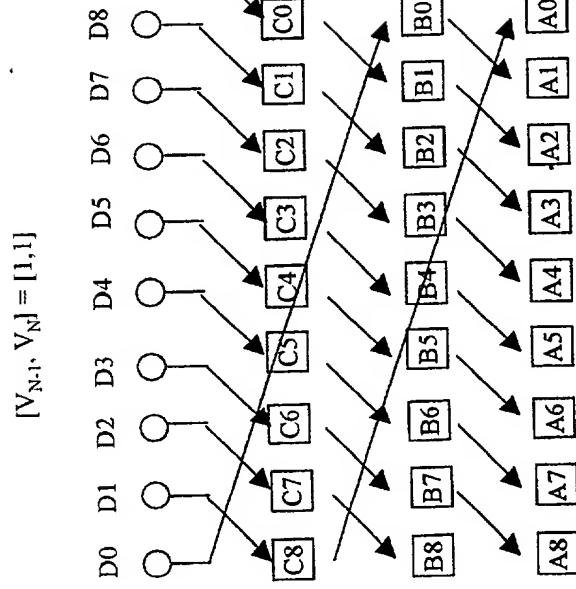


Fig 42 C

File: 00100000000000000000000000000000

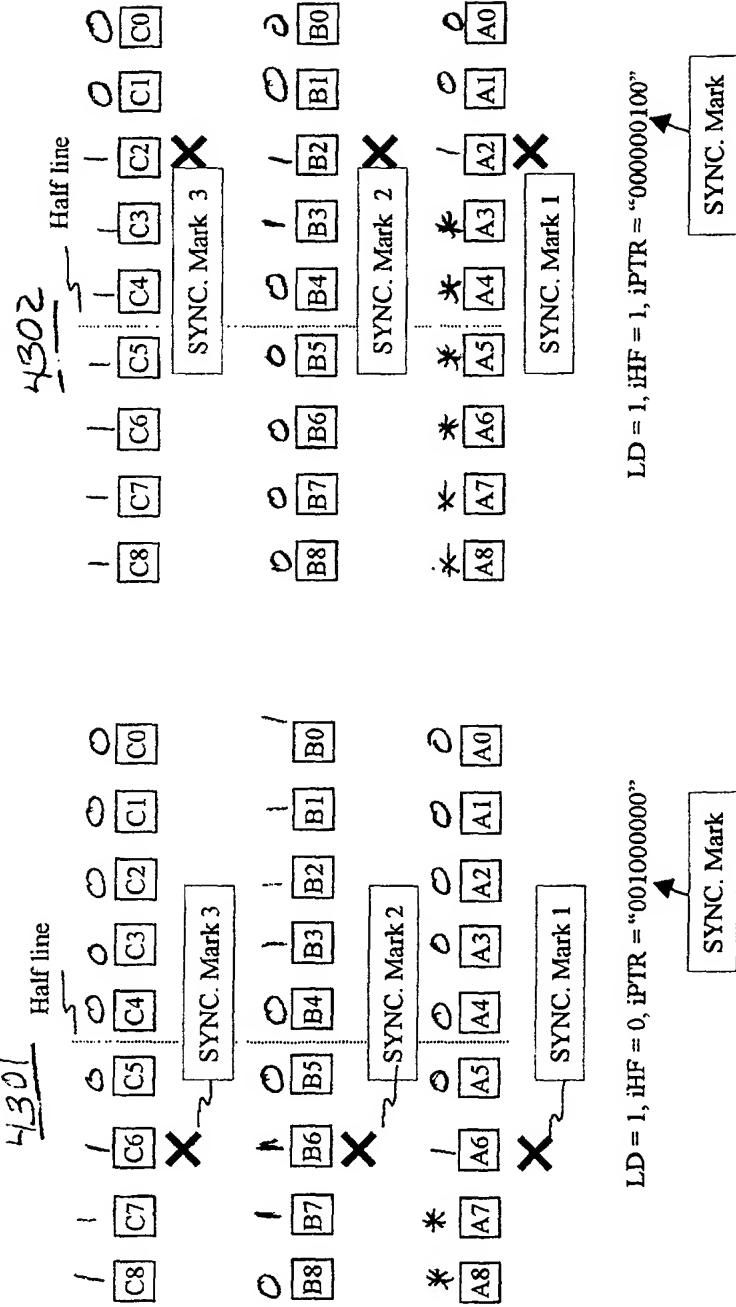
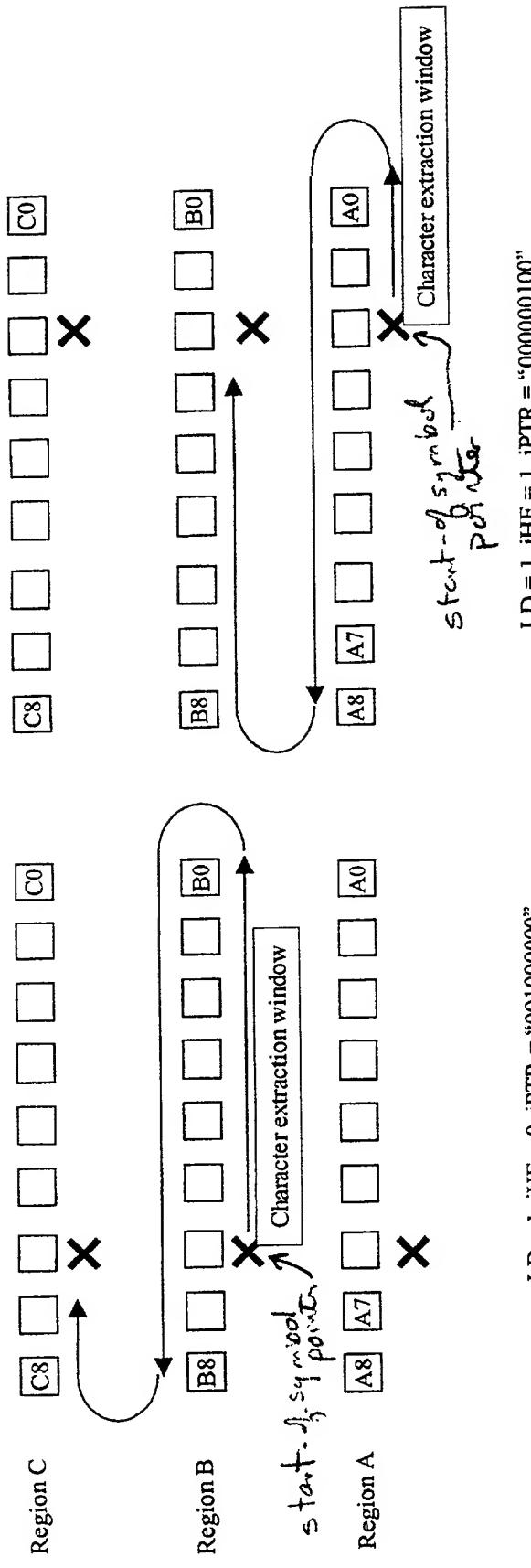


Fig. 43

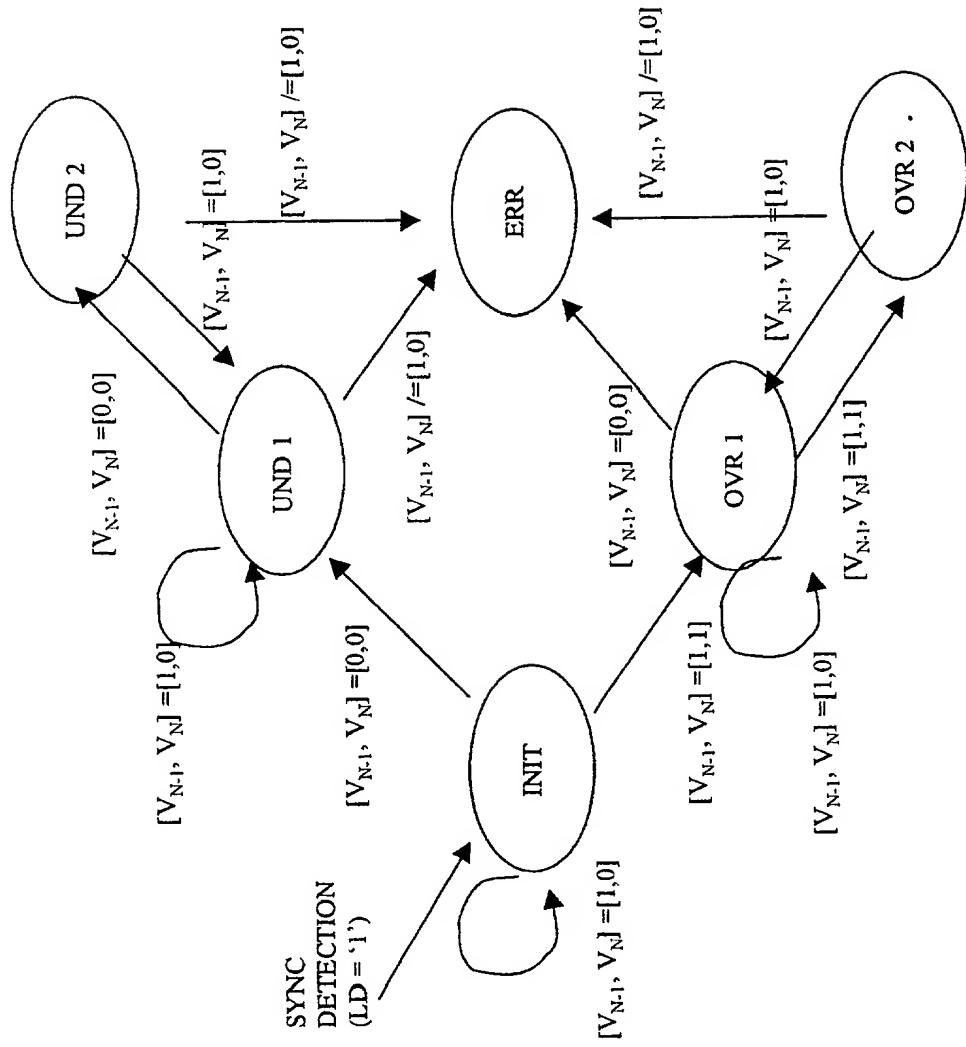
字符识别流程图



LD = 1, iHF = 0, iPTR = "001000000"

LD = 1, iHF = 1, iPTR = "0000000100"

F<sub>1</sub> S 44



F.8 45

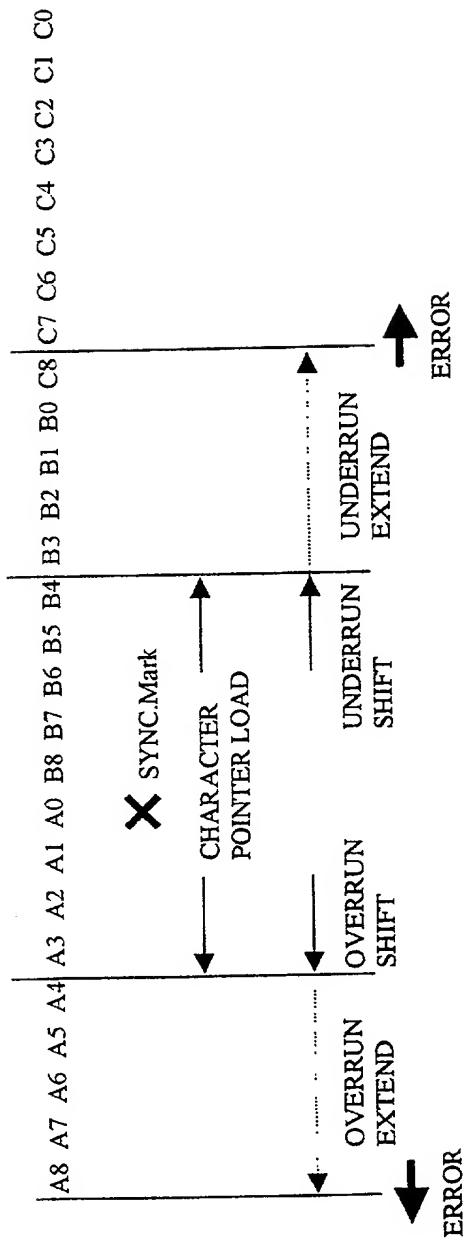


Fig 46

Figure 47B

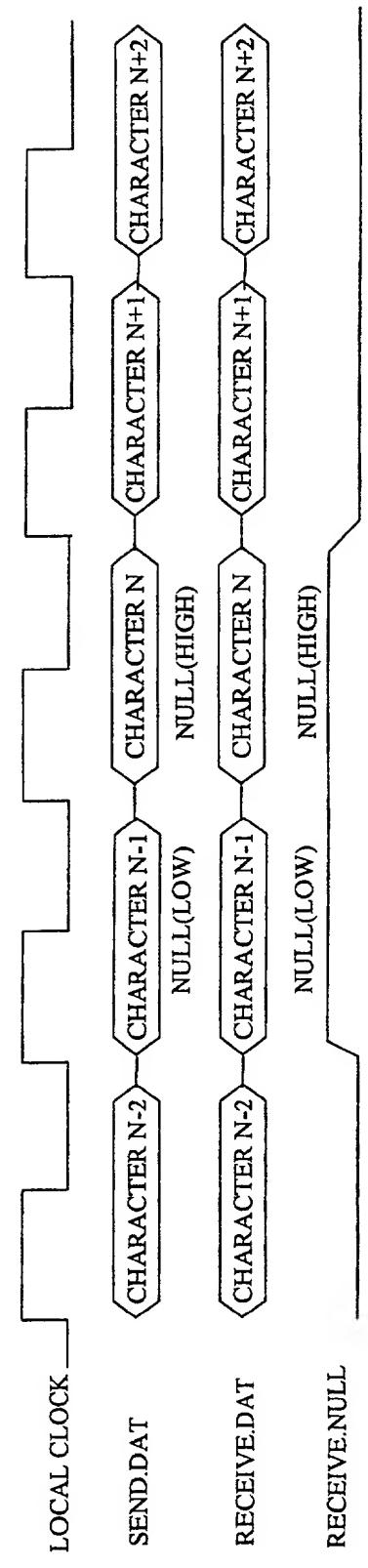
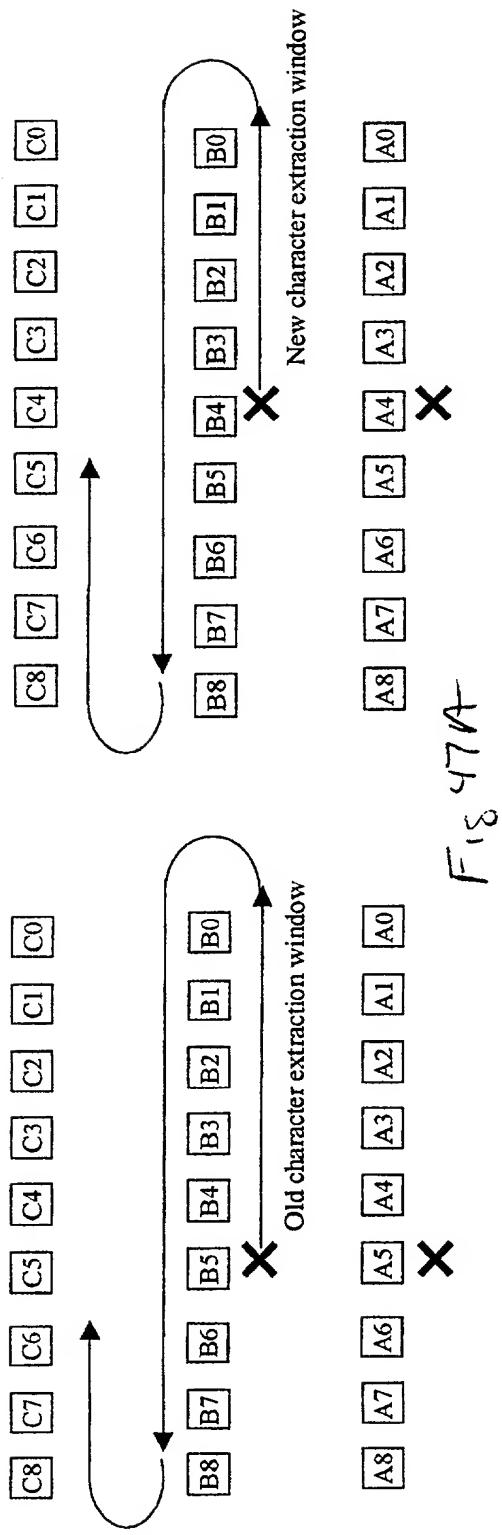


Fig 47B

Figure 48 A

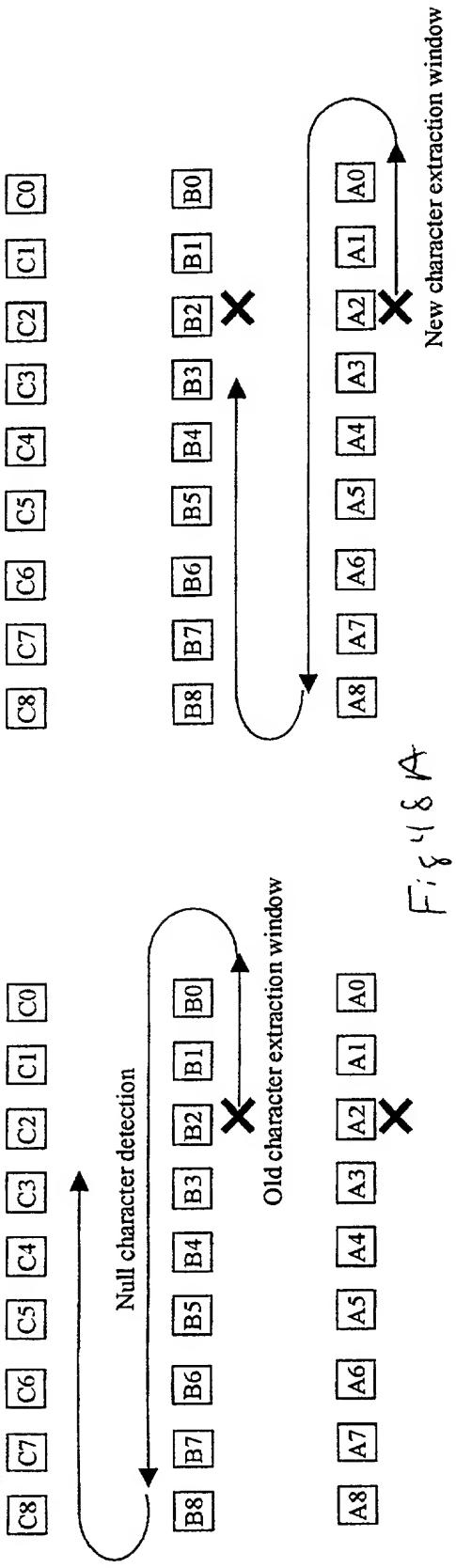


Figure 48 B

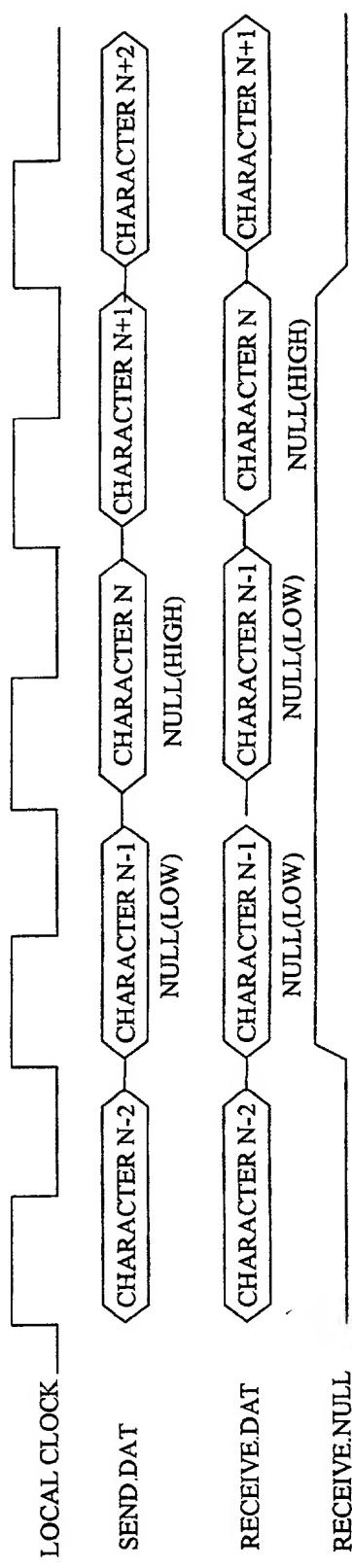


Fig. 49 A

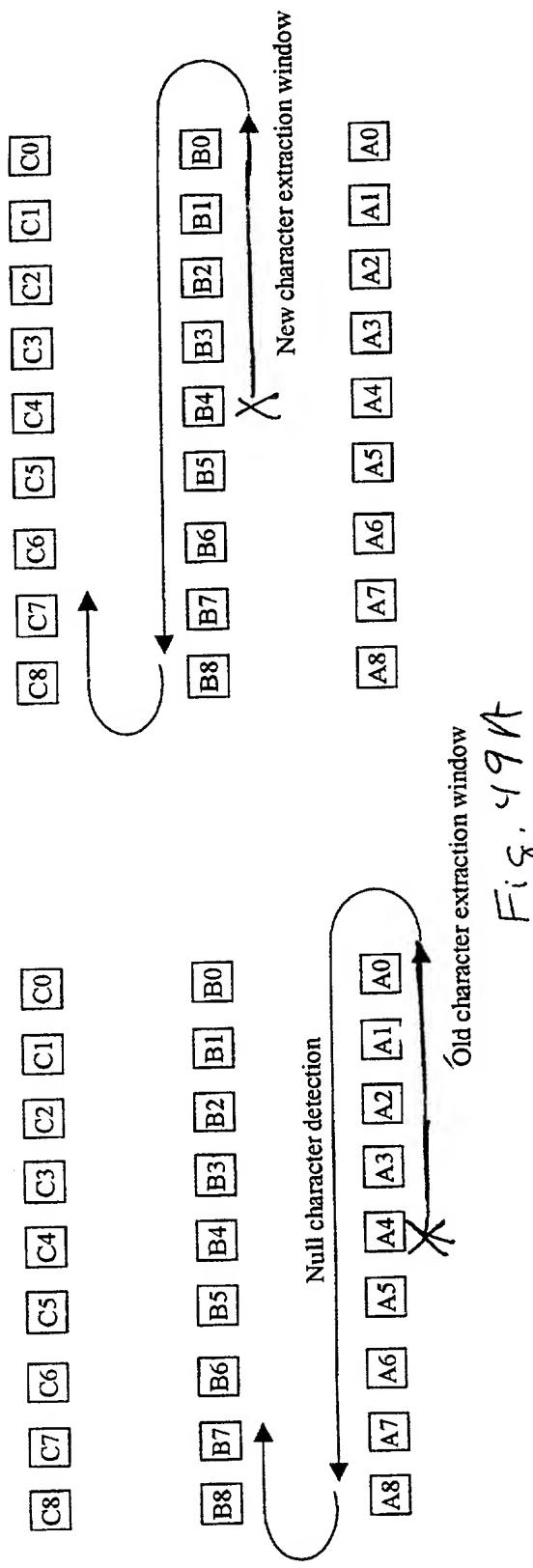


Fig. 49 A

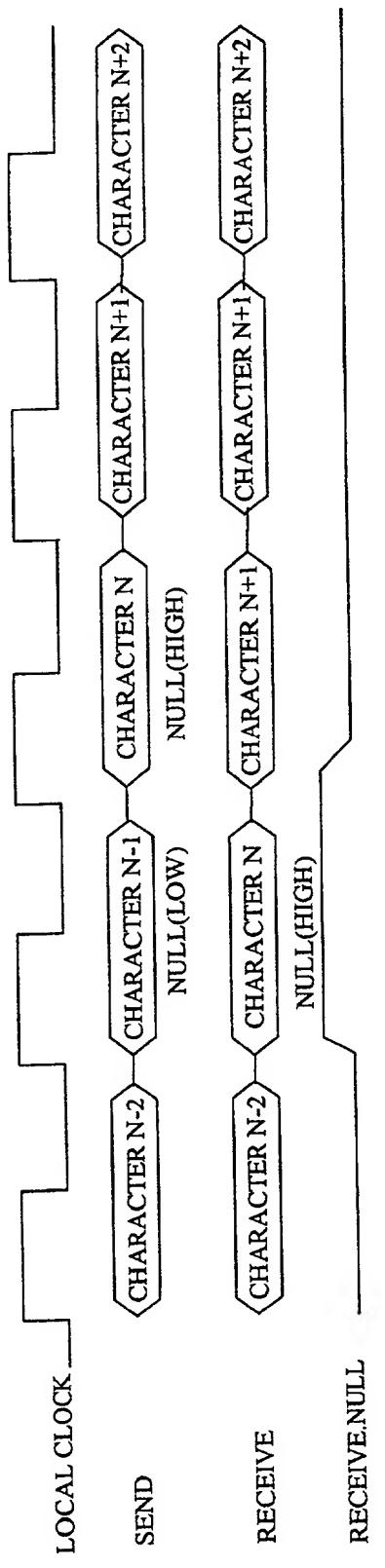


Fig. 49 B